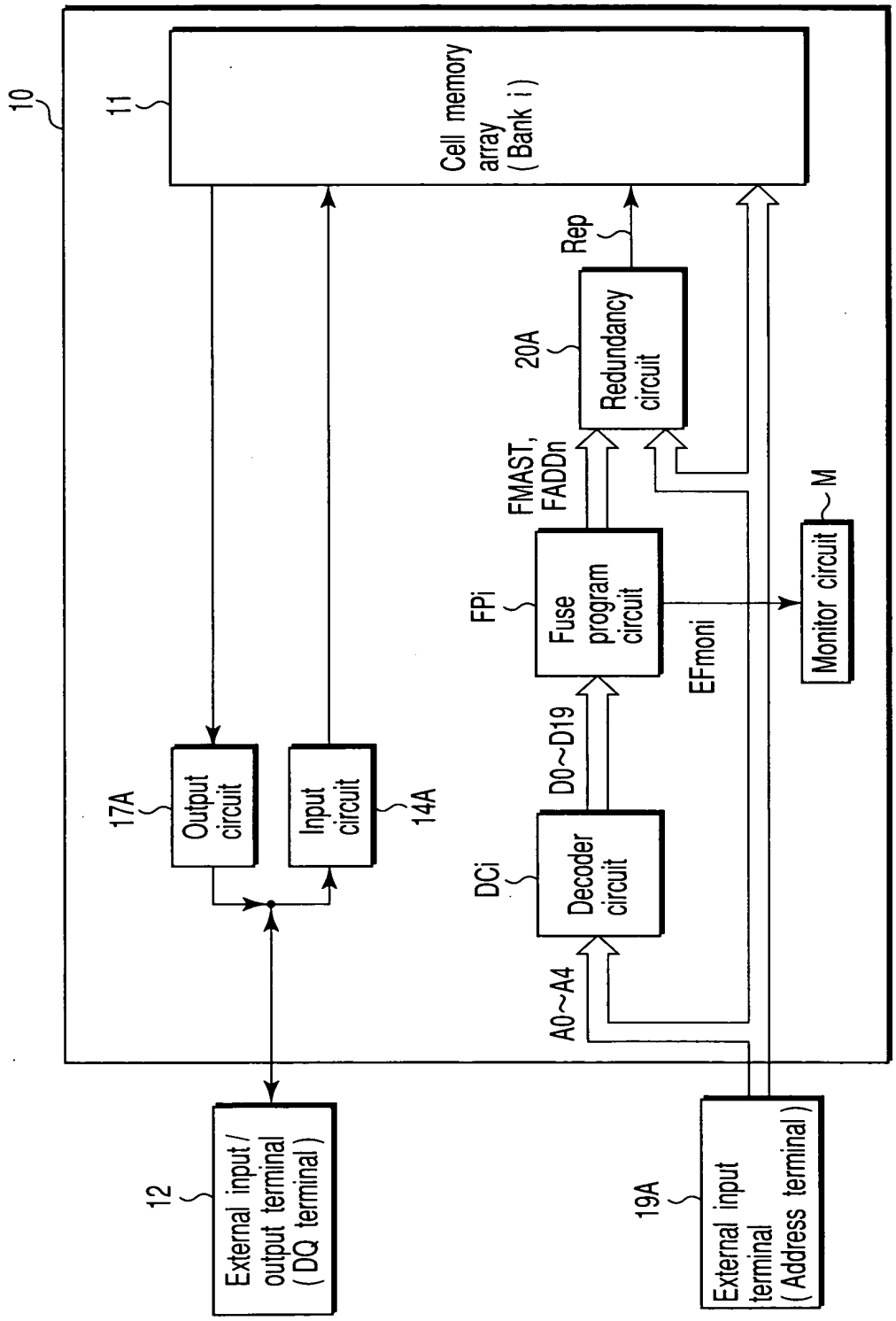

FIG. 1 (PRIOR ART)

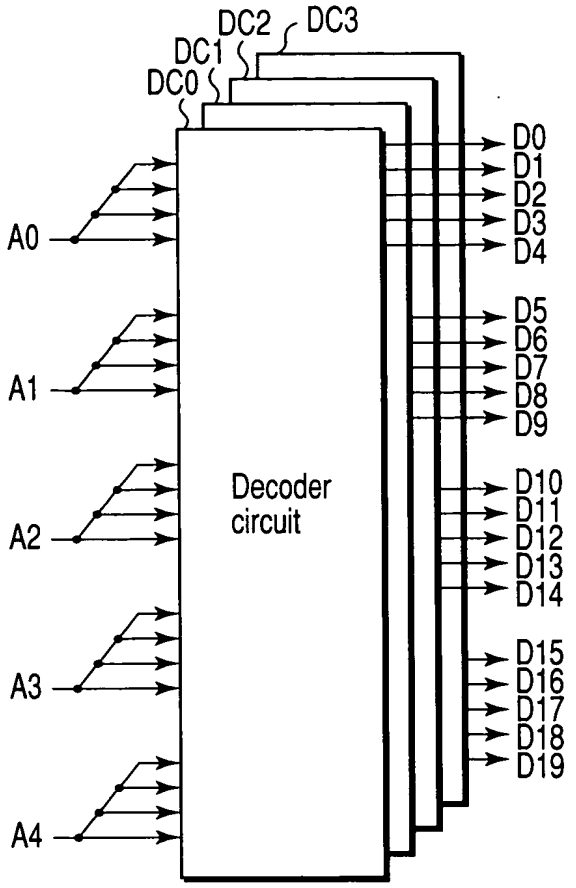

FIG. 2
(PRIOR ART)

Operating waveform during fuse programming

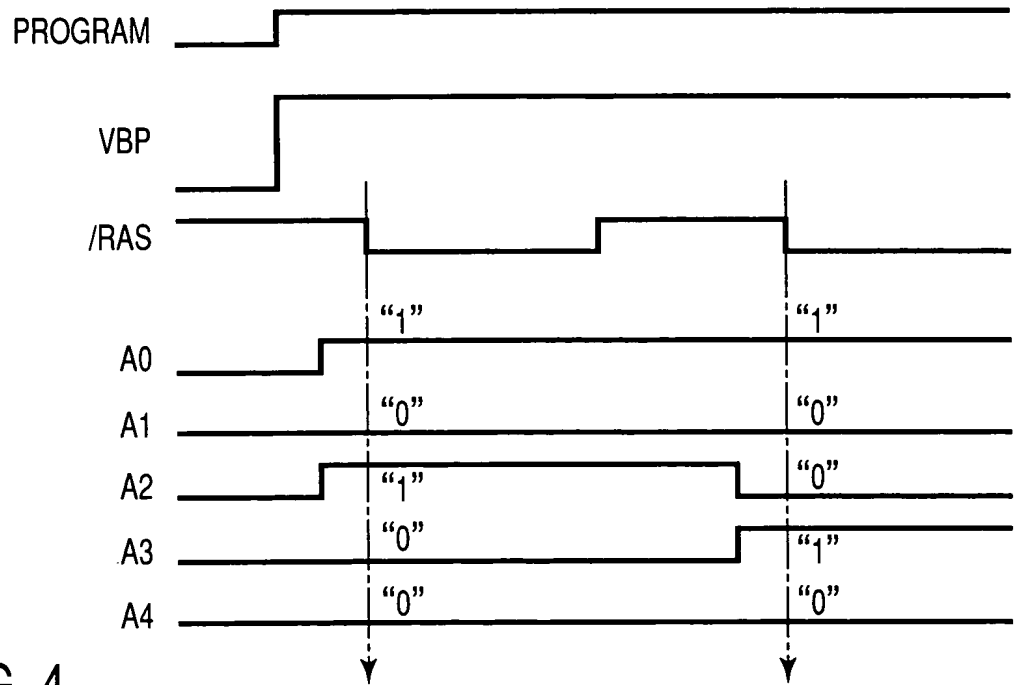

FIG. 4
(PRIOR ART)

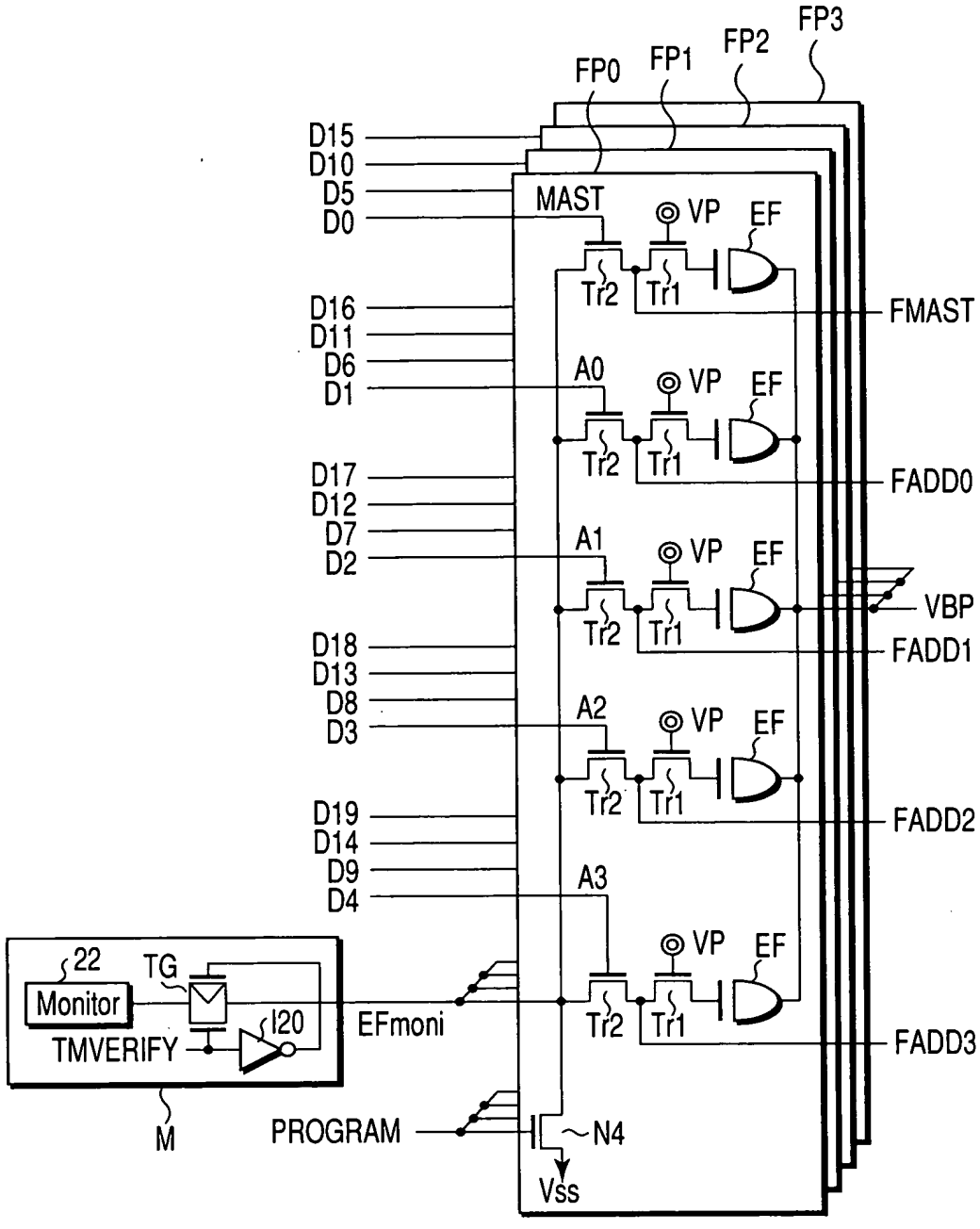

FIG. 3 (PRIOR ART)

Operating waveform during fuse verifying operation

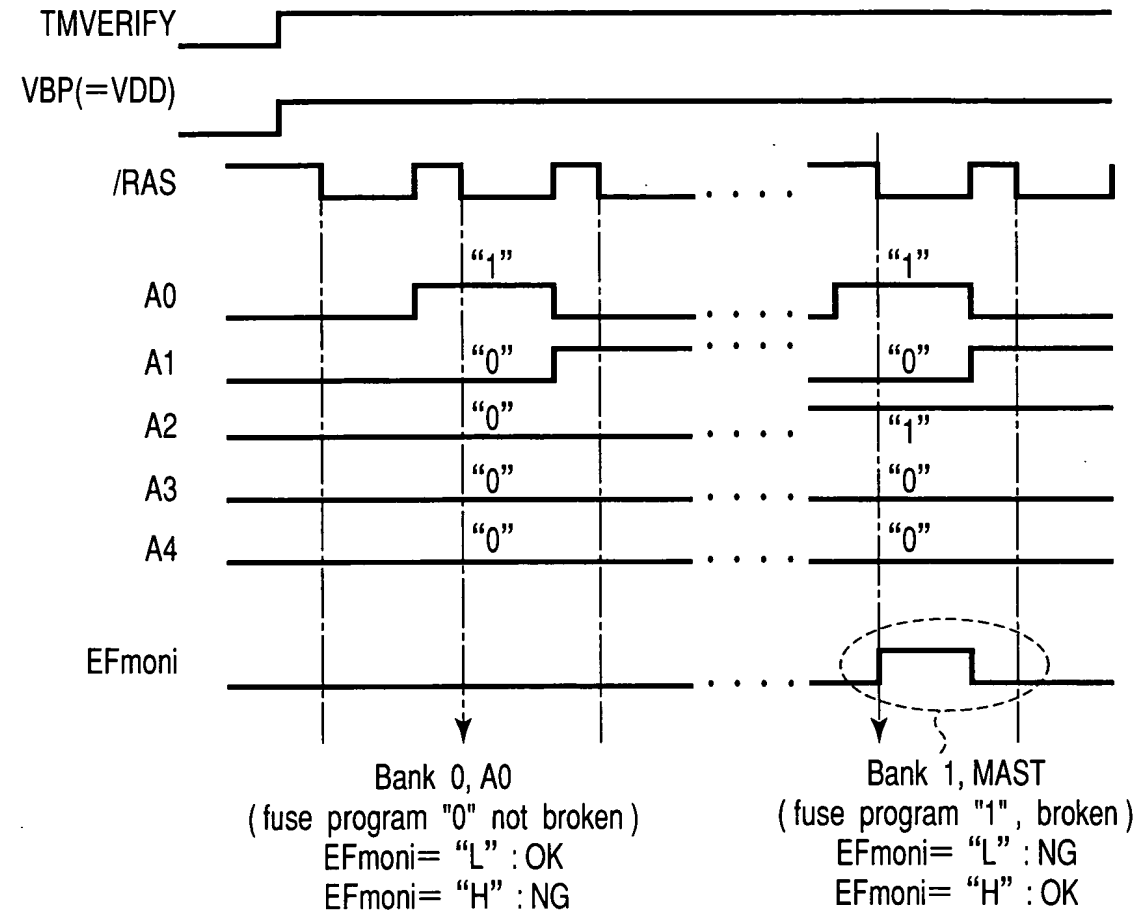

FIG. 5 (PRIOR ART)

Test flow when laser fuse is used

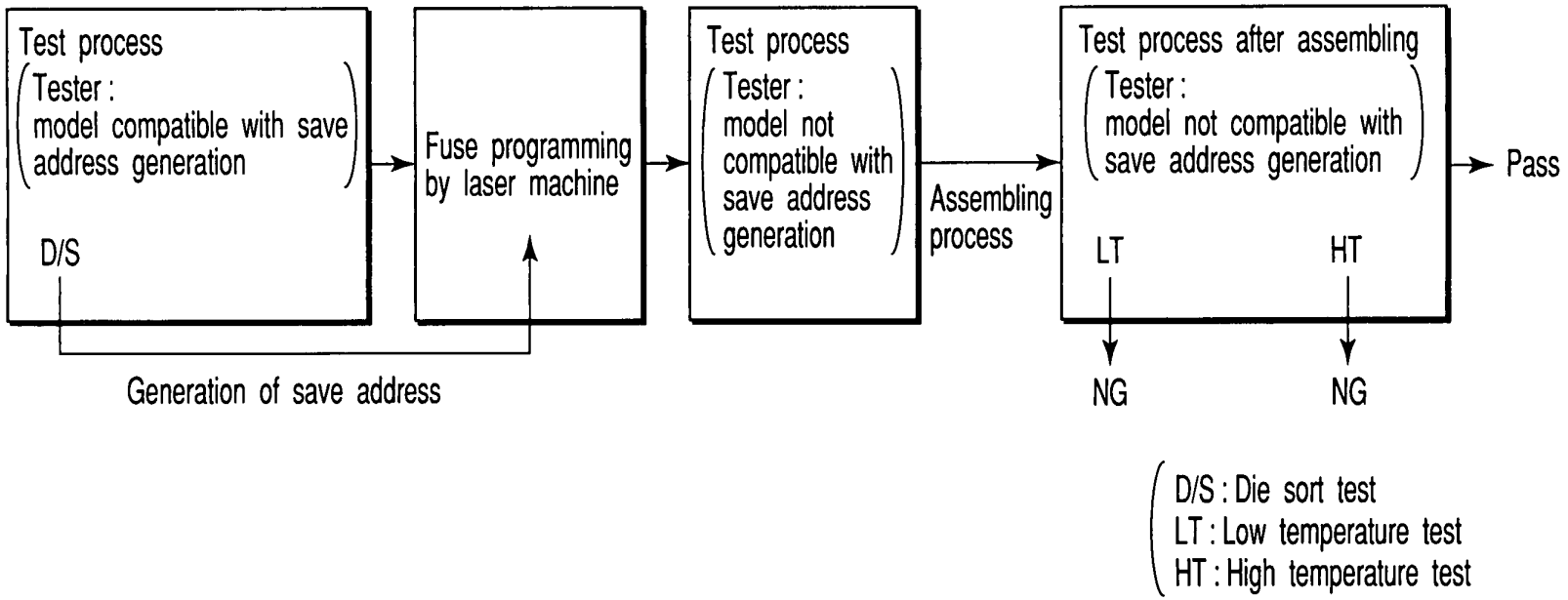

FIG. 6 (PRIOR ART)

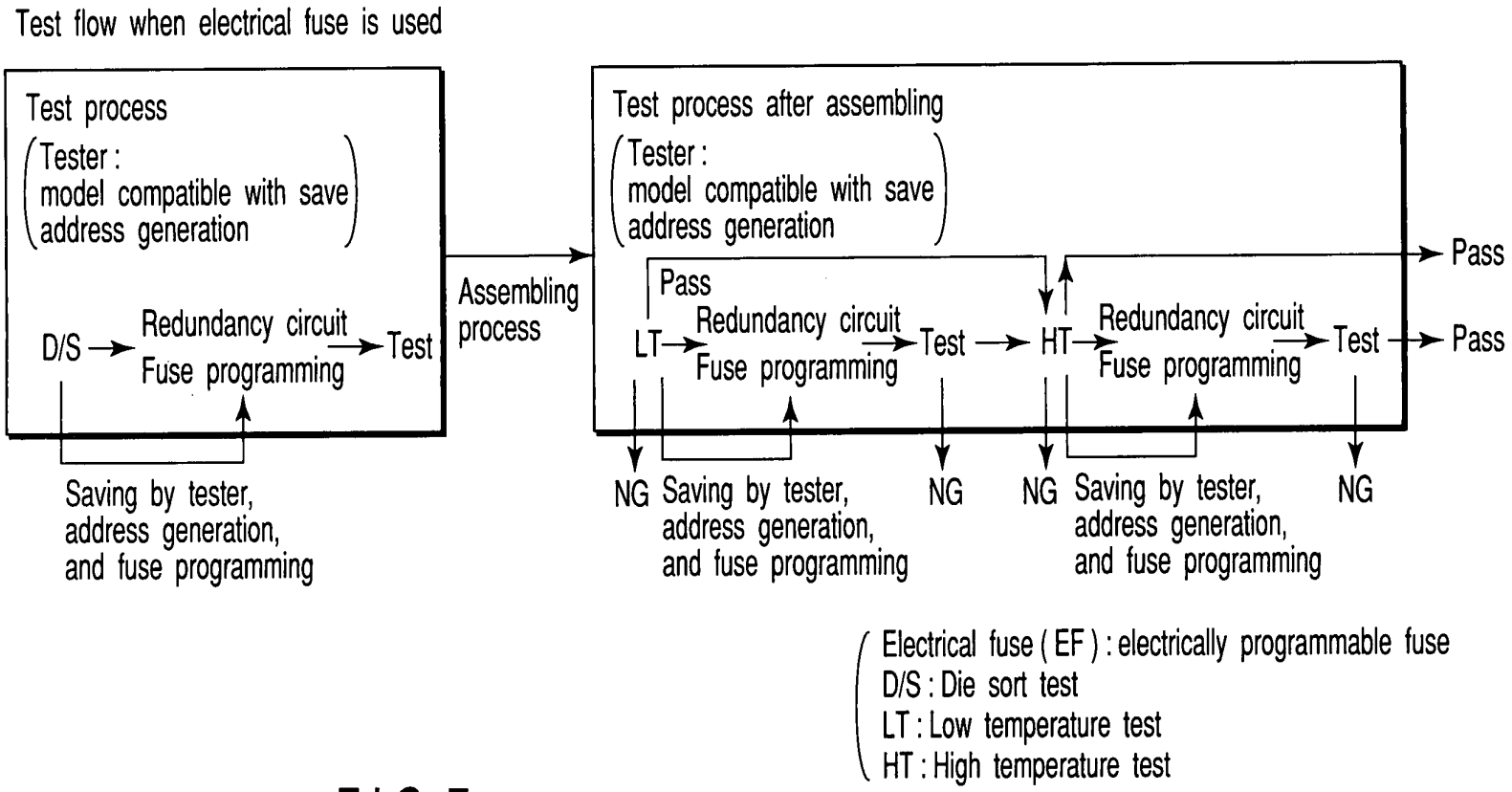

FIG. 7 (PRIOR ART)

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Eiji KOZUKA, "SEMICONDUCTOR MEMORY"
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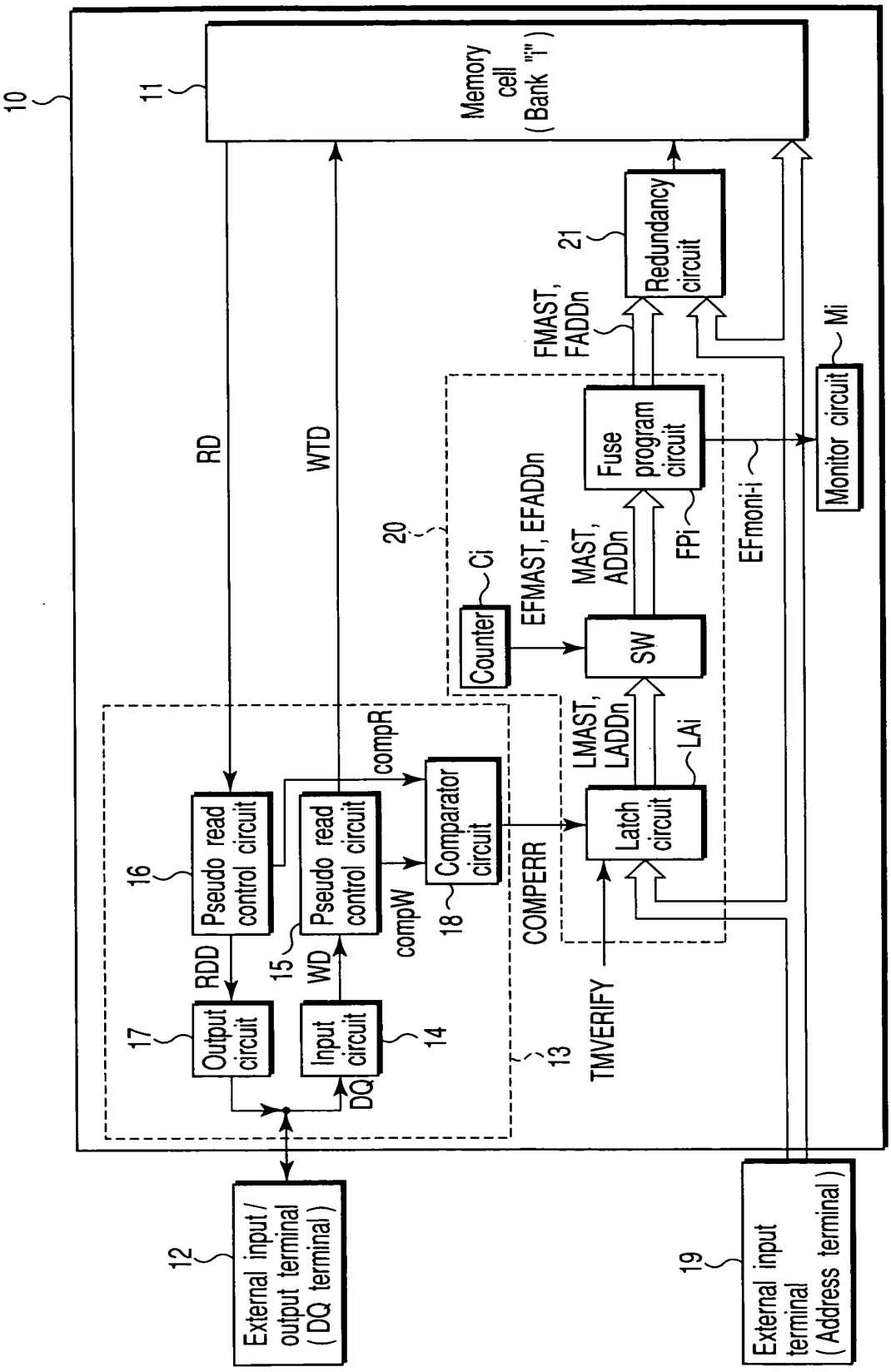

FIG. 8 (PRIOR ART)

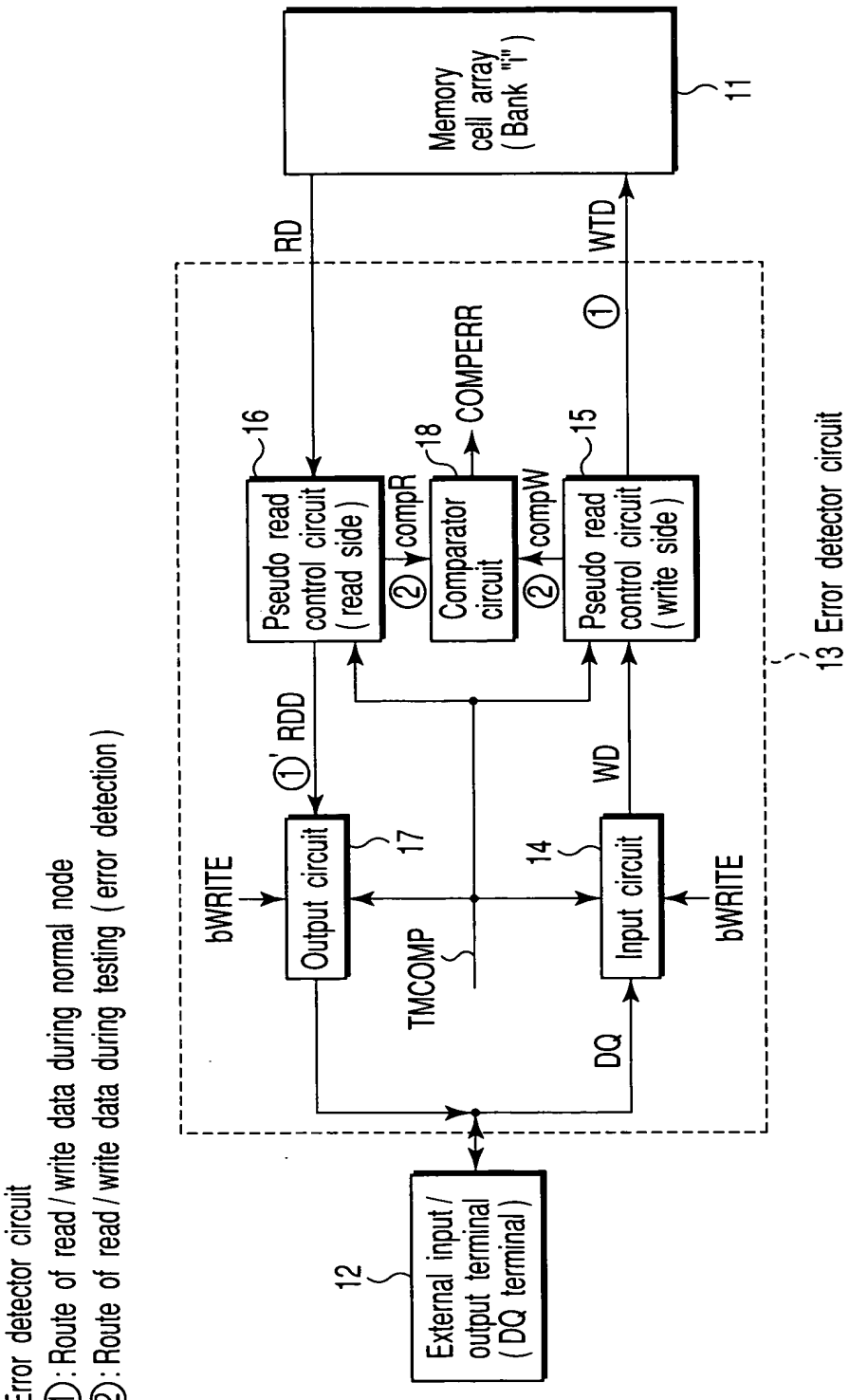
Memory cell array (Bank "i")
11
RD
WTD
16
18
COMPERR
15
Pseudo read control circuit (read side)
compR
Comparator circuit
compW
Pseudo read control circuit (write side)
① RDD
WD
bWRITE
Output circuit
17
14
Input circuit
bWRITE
TMCOMP
DQ
13 Error detector circuit
12
External input / output terminal (DQ terminal)
Error detector circuit
①: Route of read / write data during normal node
②: Route of read / write data during testing (error detection)

FIG. 9

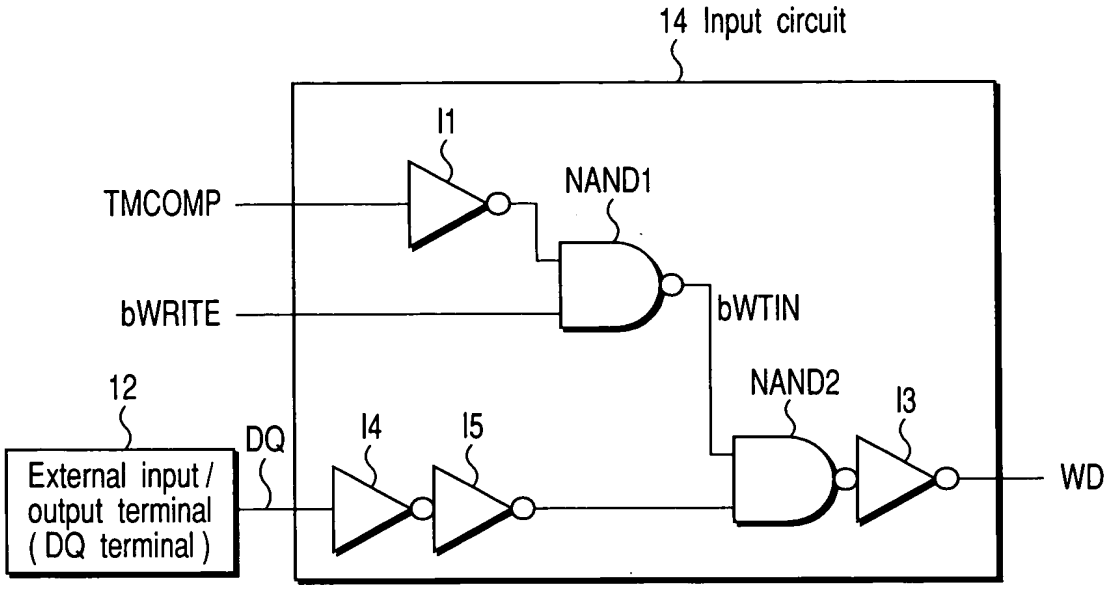
14 Input circuit
I1
NAND1
TMCOMP
bWRITE
bWTIN
NAND2
I3
12
DQ
I4
I5
External input / output terminal (DQ terminal)
WD

FIG. 10

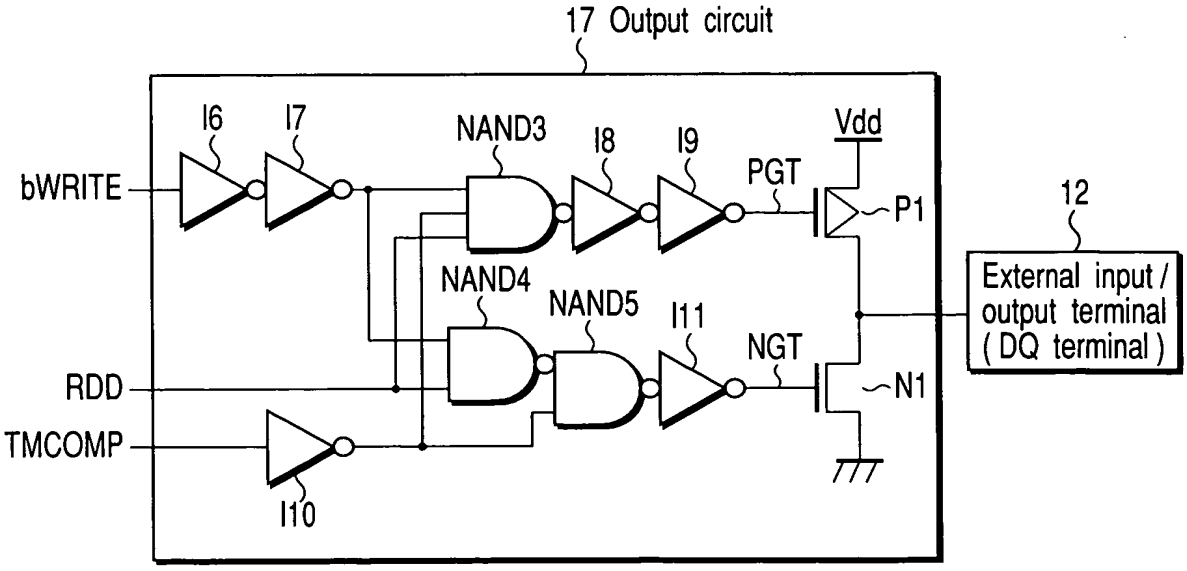
17 Output circuit
I6
I7
NAND3
I8
I9
Vdd
PGT
P1
12
bWRITE
NAND4
NAND5
I11
NGT
External input / output terminal (DQ terminal)
RDD
N1
TMCOMP
I10

FIG. 12

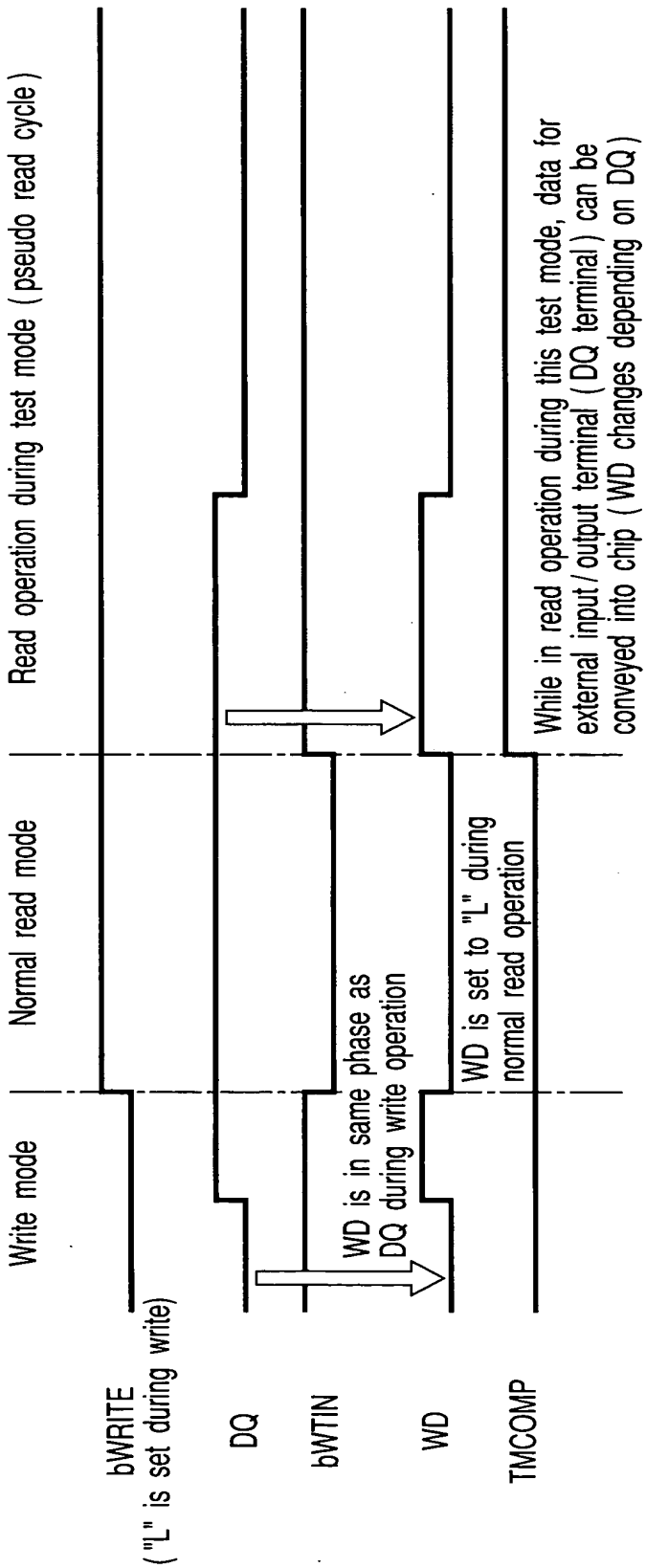
Write mode
Normal read mode
Read operation during test mode (pseudo read cycle)
bWRITE
("L" is set during write)
DQ
bWTIN
WD
TMCOMP
WD is in same phase as DQ during write operation
WD is set to "L" during normal read operation
While in read operation during this test mode, data for external input / output terminal (DQ terminal) can be conveyed into chip (WD changes depending on DQ)

FIG. 11

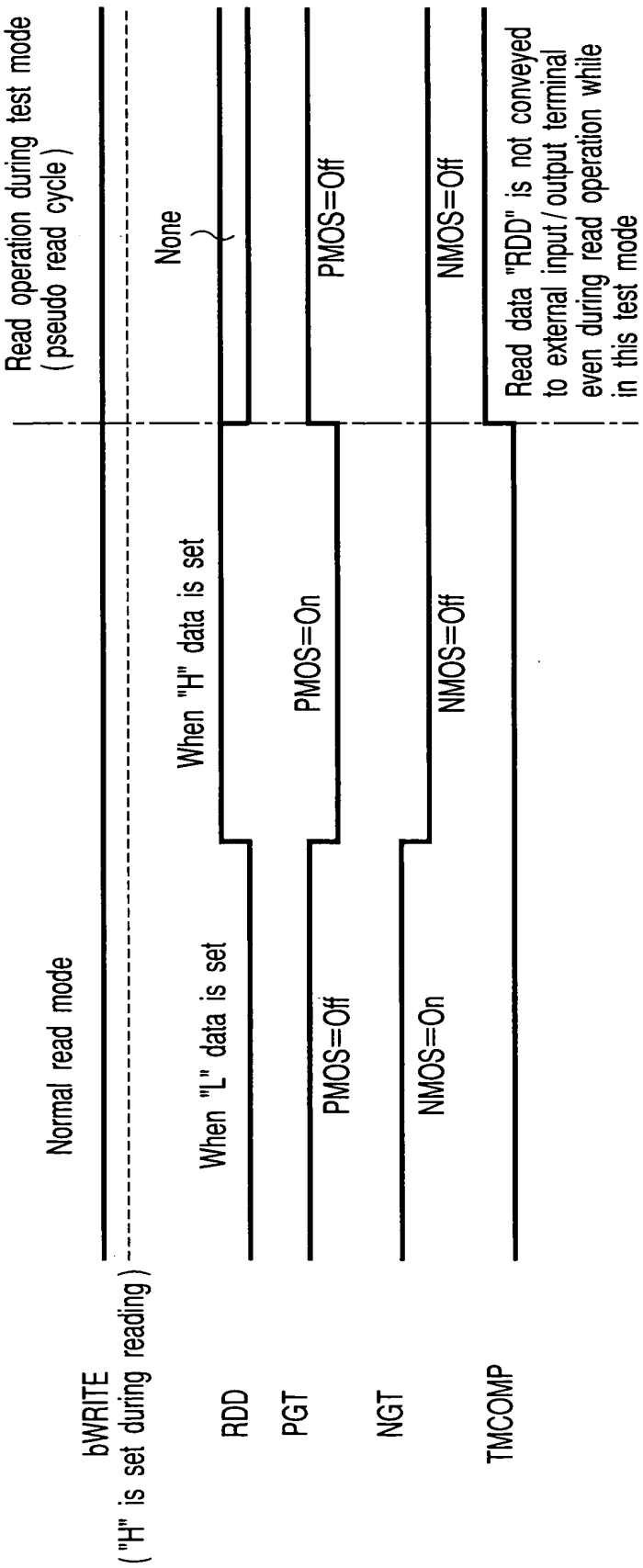
Normal read mode
Read operation during test mode
(pseudo read cycle)
bWRITE
("H" is set during reading)
None
When "H" data is set
When "L" data is set
RDD
PGT
NGT
TMCOMP
PMOS=On
PMOS=Off
NMOS=Off
NMOS=On
PMOS=Off
NMOS=Off
Read data "RDD" is not conveyed to external input/output terminal even during read operation while in this test mode

FIG. 13

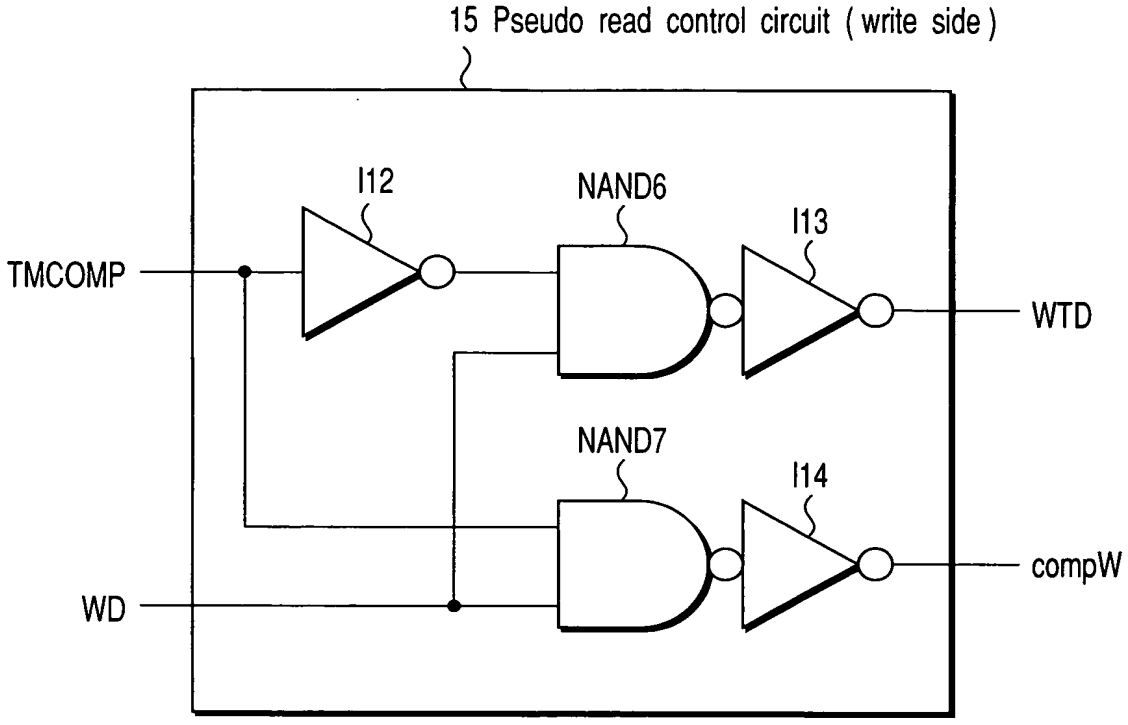
15 Pseudo read control circuit (write side)
I12
NAND6
I13
TMCOMP
WTD
NAND7
I14
compW
WD

FIG. 14

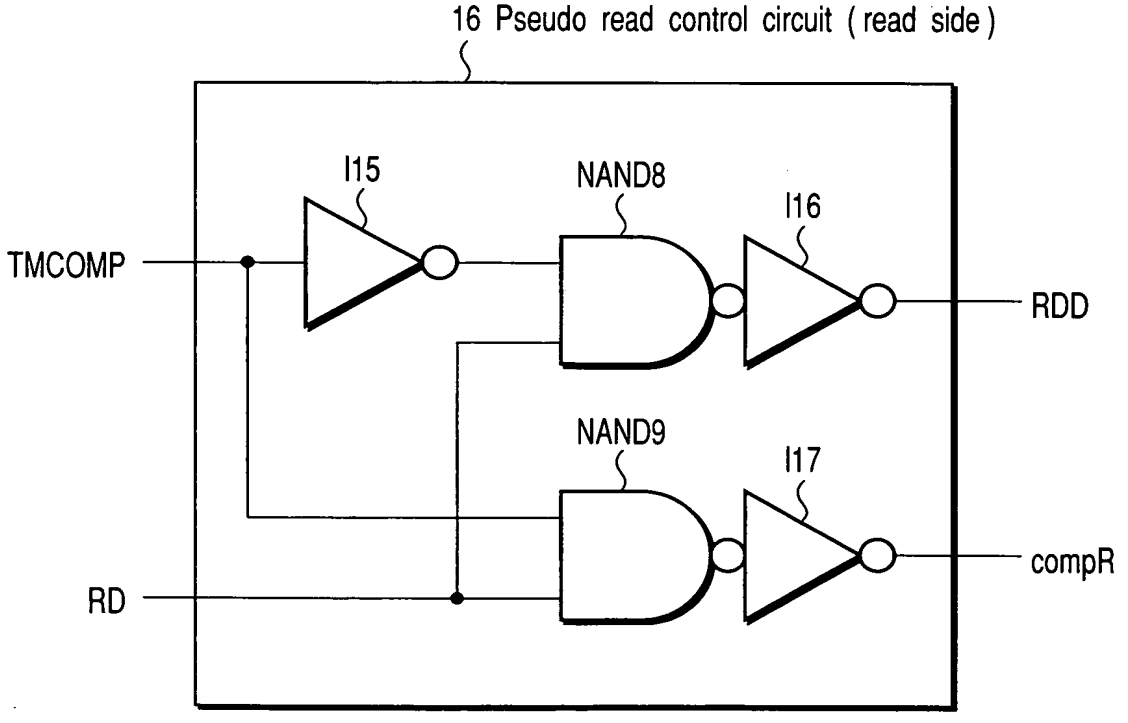
16 Pseudo read control circuit (read side)
I15
NAND8
I16
TMCOMP
RDD
NAND9
I17
compR
RD

FIG. 15

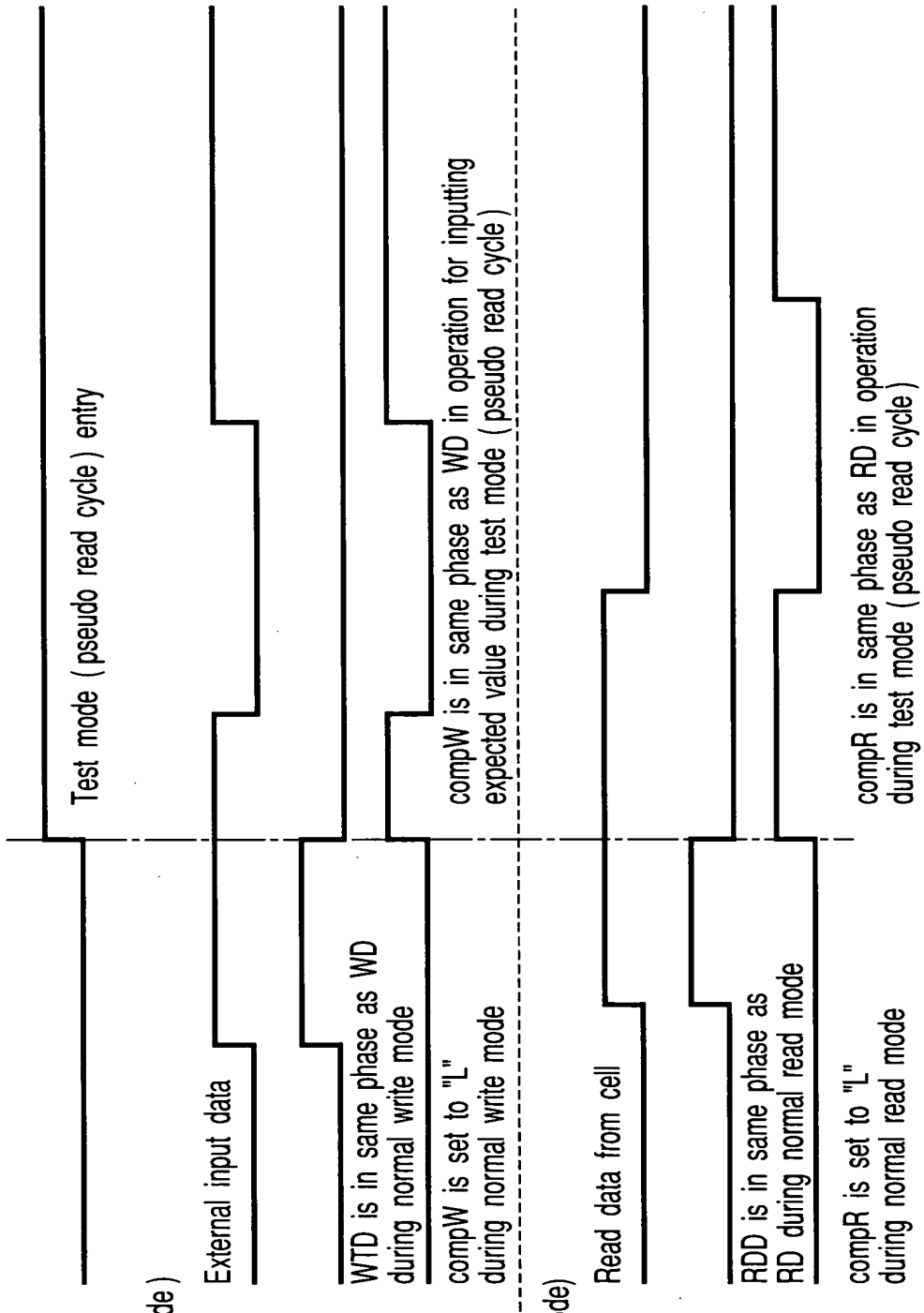
TMCOMP
Test mode (pseudo read cycle) entry
(During Write mode)
WD
External input data
WTD
WTD is in same phase as WD during normal write mode
compW
compW is set to "L" during normal write mode
compW is in same phase as WD in operation for inputting expected value during test mode (pseudo read cycle)
(During Read mode)
RD
Read data from cell
RDD
RDD is in same phase as RD during normal read mode
compR
compR is set to "L" during normal read mode
compR is in same phase as RD in operation during test mode (pseudo read cycle)

FIG. 16

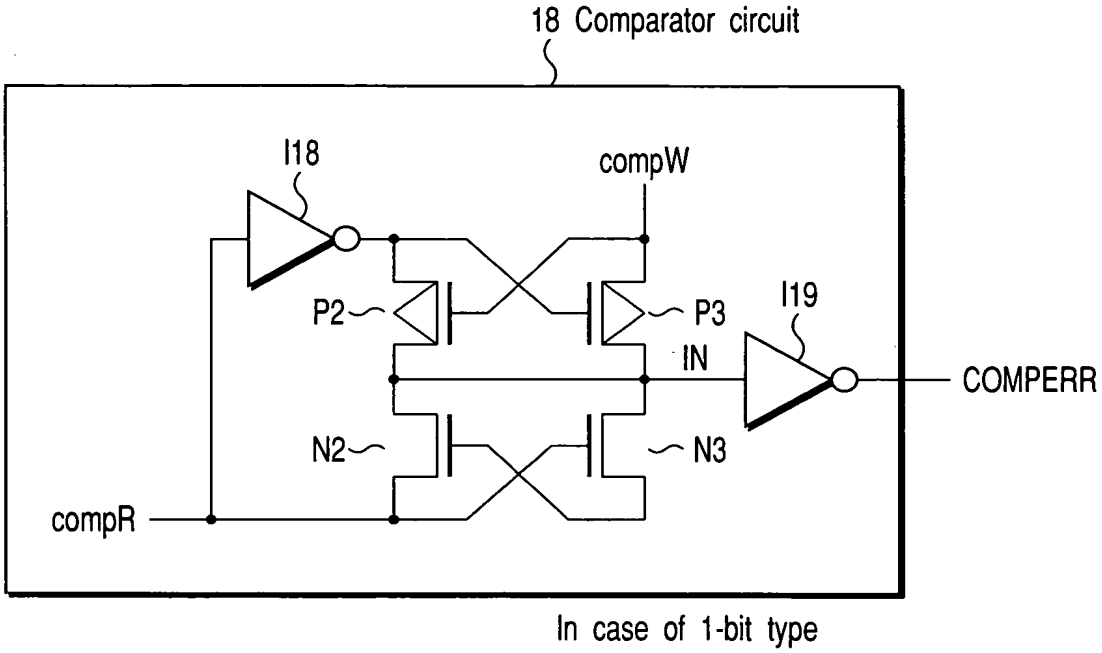
18 Comparator circuit
I18
compW
P2
P3
I19
IN
COMPERR
N2
N3
compR
In case of 1-bit type

FIG. 17

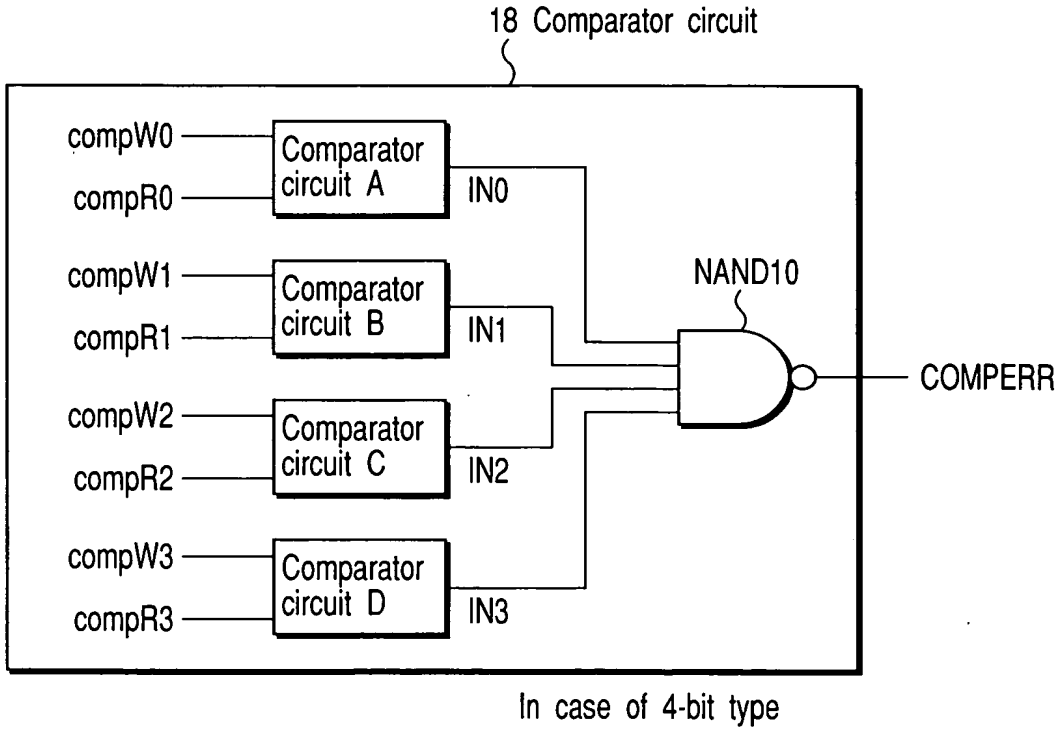
18 Comparator circuit
compW0
compR0
Comparator circuit A
IN0
compW1
compR1
Comparator circuit B
IN1
NAND10
compW2
compR2
Comparator circuit C
IN2
COMPERR
compW3
compR3
Comparator circuit D
IN3
In case of 4-bit type

FIG. 18

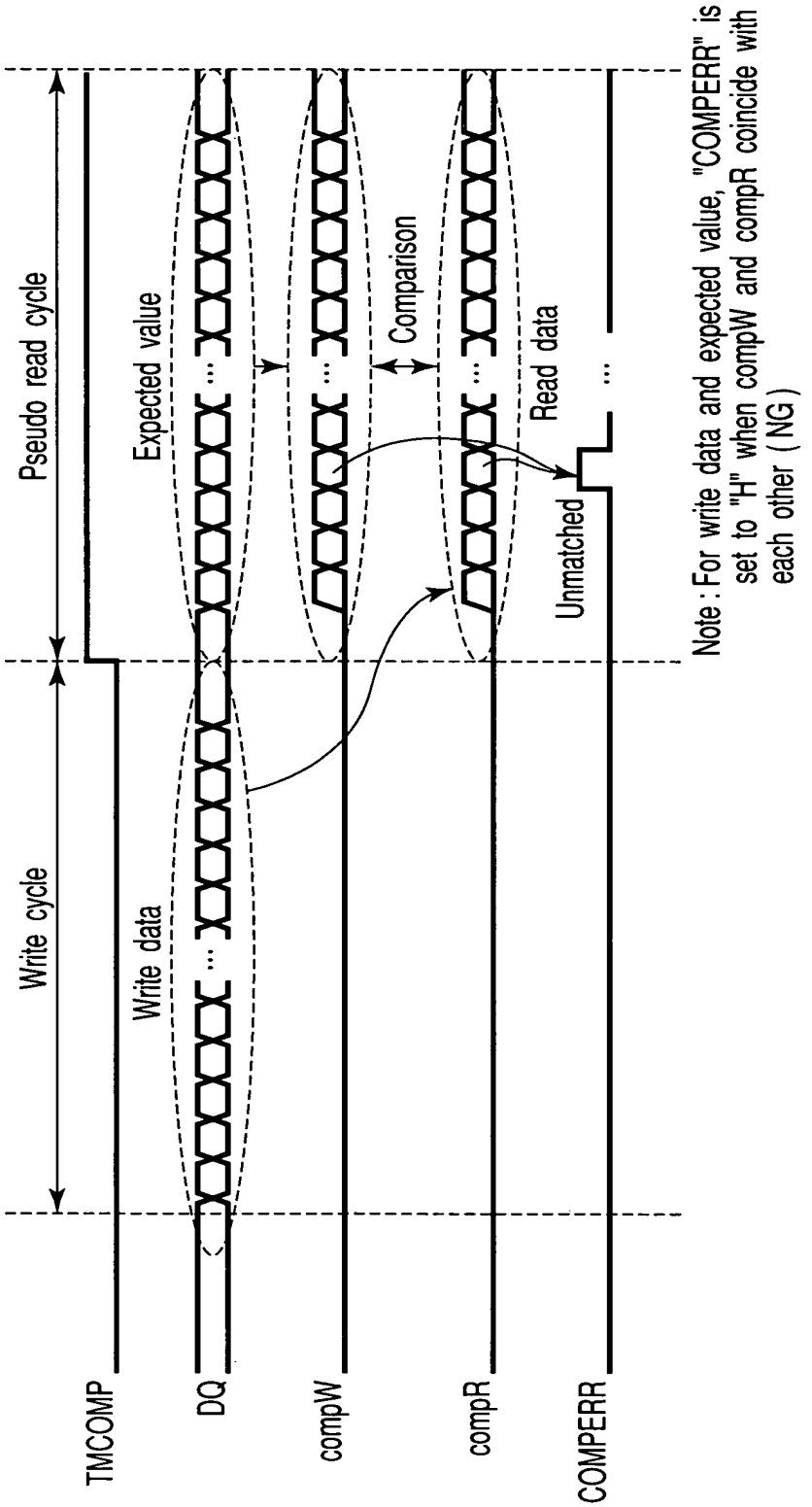
Pseudo read cycle
Write cycle
Expected value
Write data
Comparison
Read data
Unmatched
Note : For write data and expected value, "COMPERR" is set to "H" when compW and compR coincide with each other (NG)
TMCOMP
DQ
compW
compR
COMPERR

FIG. 19

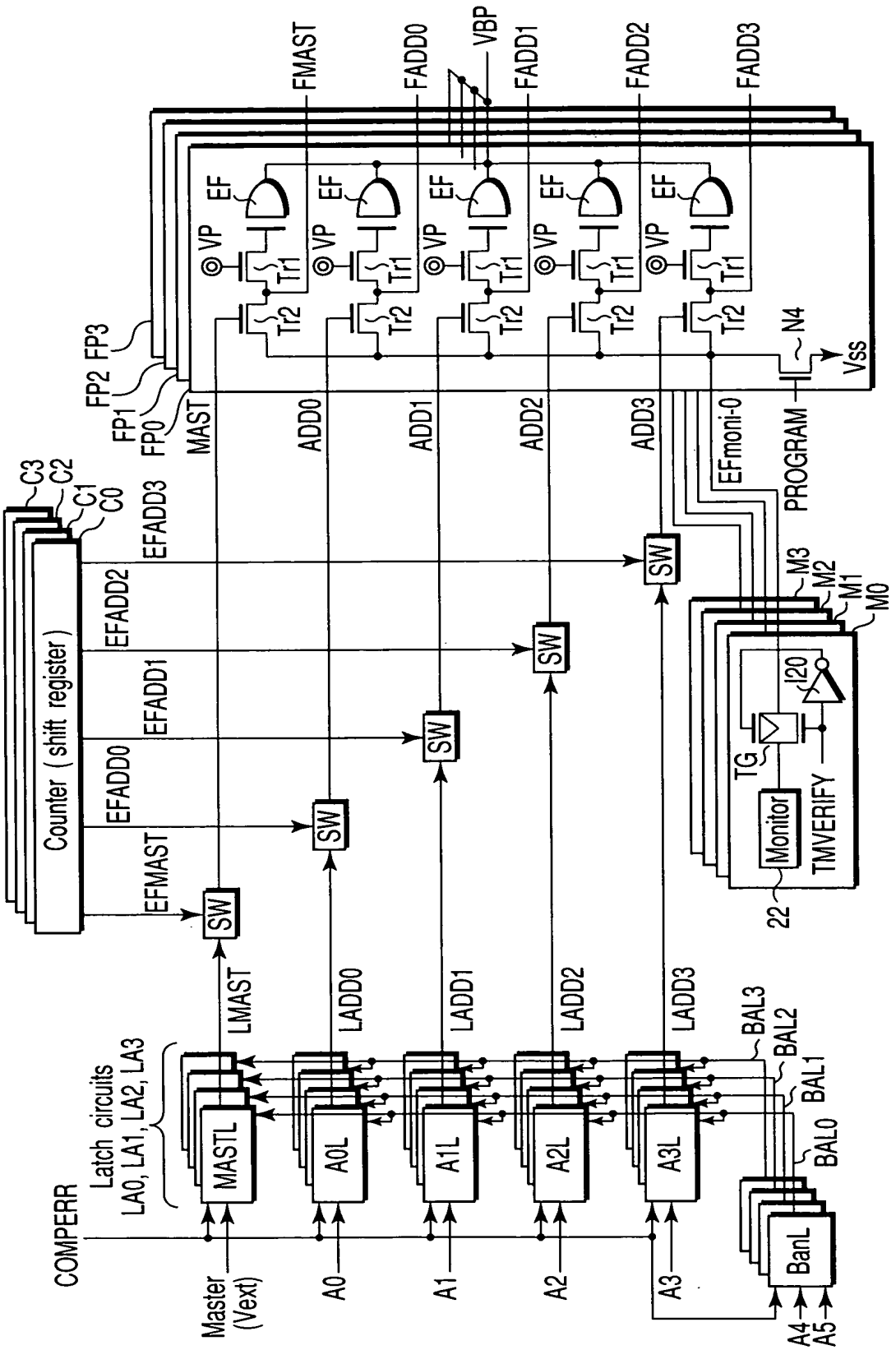
FMAST
FADD0
VBP
FADD1
FADD2
FADD3
EF
VP
Tr1
Tr2
FP3
FP2
FP1
FP0
MAST
N4
Vss
ADD0
ADD1
ADD2
ADD3
EFmoni-0
PROGRAM
C3
C2
C1
C0
EFADD3
EFADD2
EFADD1
EFADD0
EFMAST
Counter (shift register)
SW
M3
M2
M1
M0
I20
TG
Monitor
TMVERIFY
22
LMAST
LADD0
LADD1
LADD2
LADD3
BAL3
BAL2
BAL1
BAL0
Latch circuits
LA0, LA1, LA2, LA3
MASTL
A0L
A1L
A2L
A3L
BanL
COMPERR
Master
(Vext)
A0
A1
A2
A3
A4
A5

FIG. 20

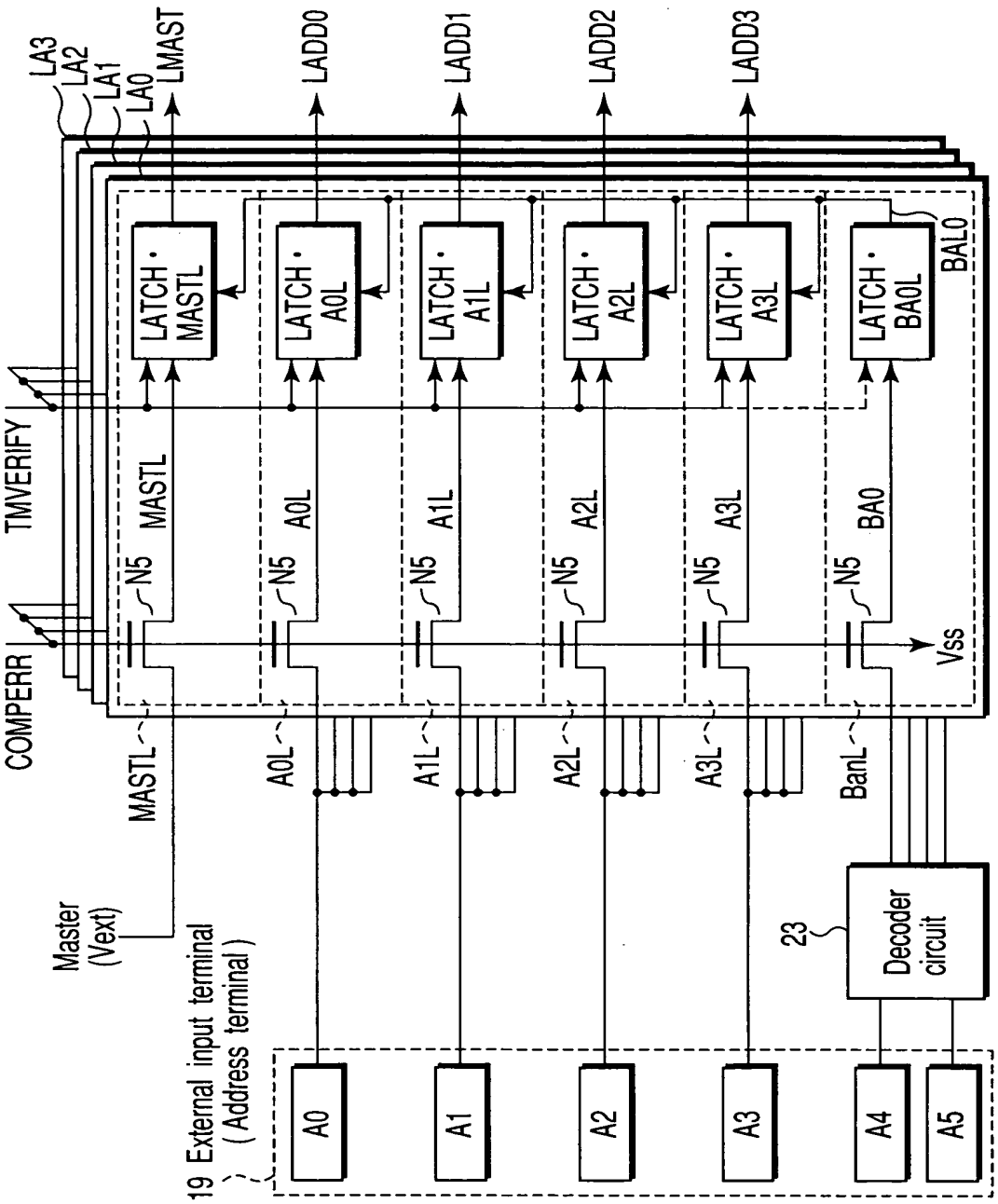
LA3
LA2
LA1
LA0
LMAST
LADD0
LADD1
LADD2
LADD3
LATCH · MASTL
LATCH · A0L
LATCH · A1L
LATCH · A2L
LATCH · A3L
LATCH · BA0L
BAL0
TMVERIFY
COMPERR
MASTL
A0L
A1L
A2L
A3L
BA0
N5
Vss
MASTL
A0L
A1L
A2L
A3L
BanL
Master (Vext)
19 External input terminal (Address terminal)
23
Decoder circuit
A0
A1
A2
A3
A4
A5

FIG. 21

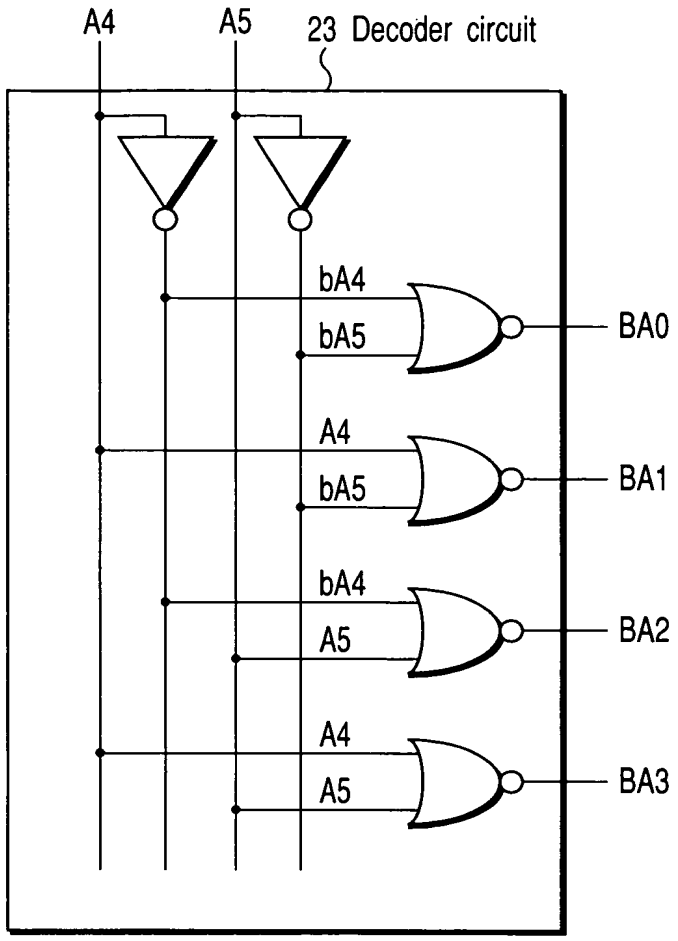
A4
A5
23 Decoder circuit
bA4
bA5
BA0
A4
bA5
BA1
bA4
A5
BA2
A4
A5
BA3

FIG. 22

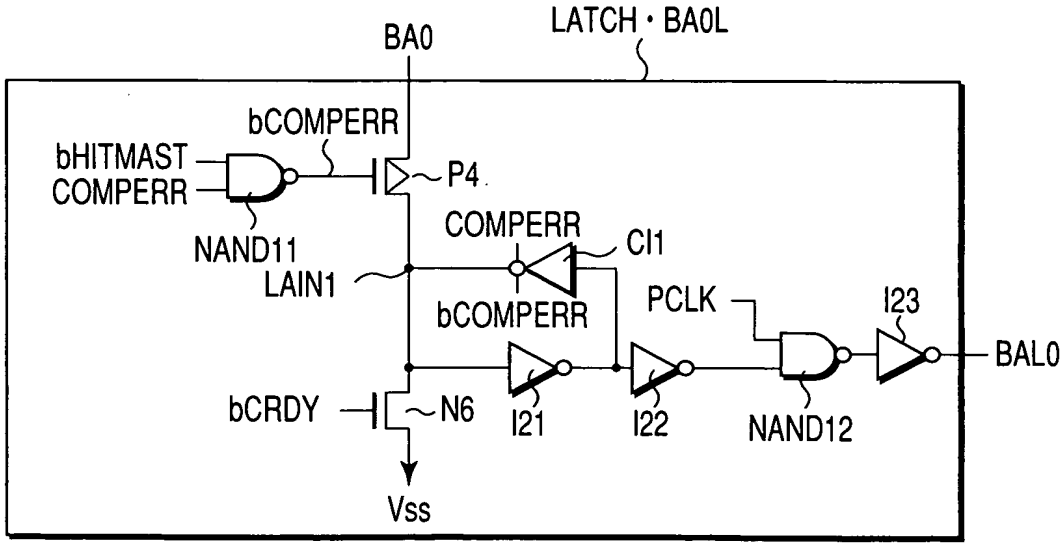
BA0
LATCH · BA0L
bCOMPERR
bHITMAST
COMPERR
P4
NAND11
COMPERR
CI1
LAIN1
bCOMPERR
PCLK
I23
BAL0
bCRDY
N6
I21
I22
NAND12
Vss

FIG. 24

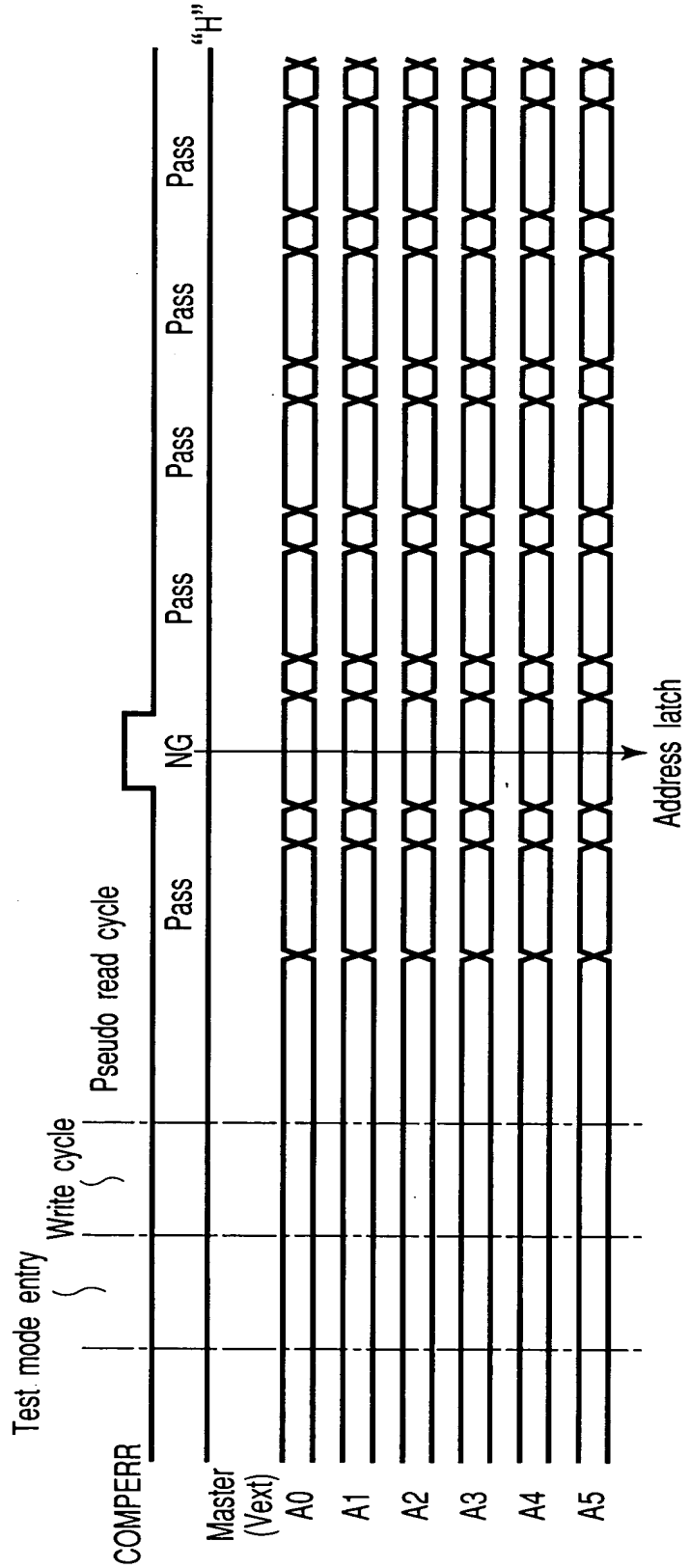
"H"
Pass
Pass
Pass
Pass
NG
Pass
Pseudo read cycle
Write cycle
Test mode entry
COMPERR
Master (Vext)
A0
A1
A2
A3
A4
A5
Address latch

FIG. 23

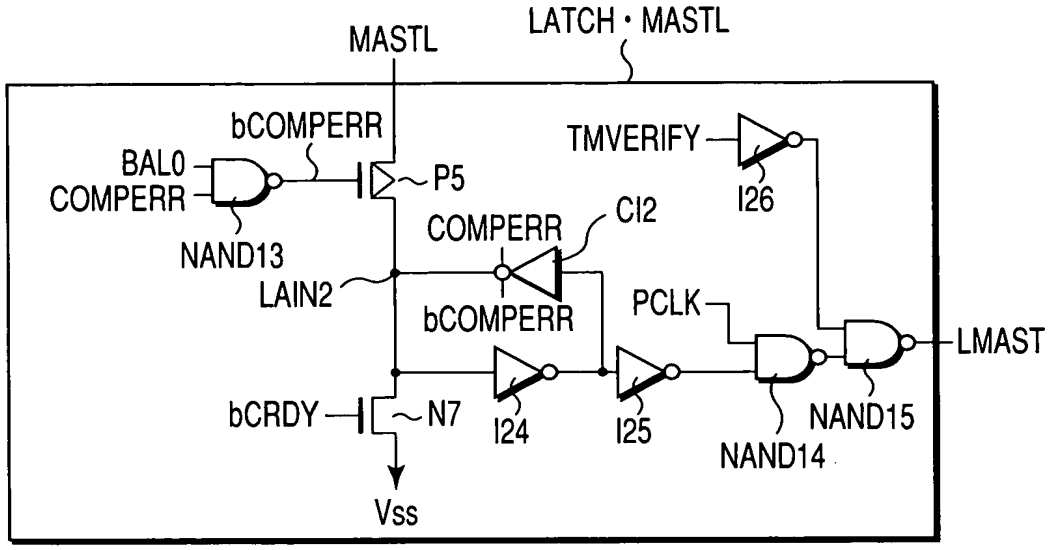

FIG. 25

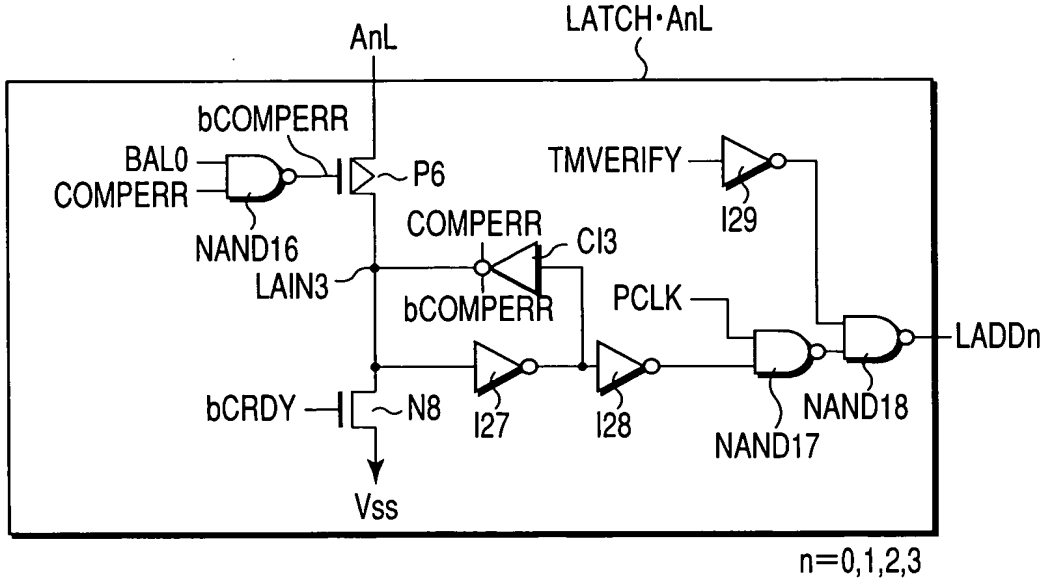

FIG. 26

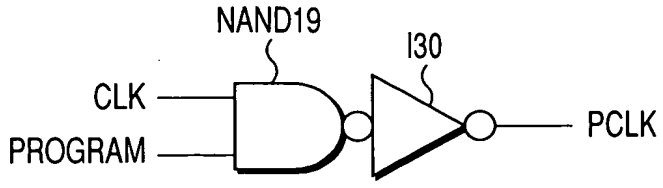

FIG. 27

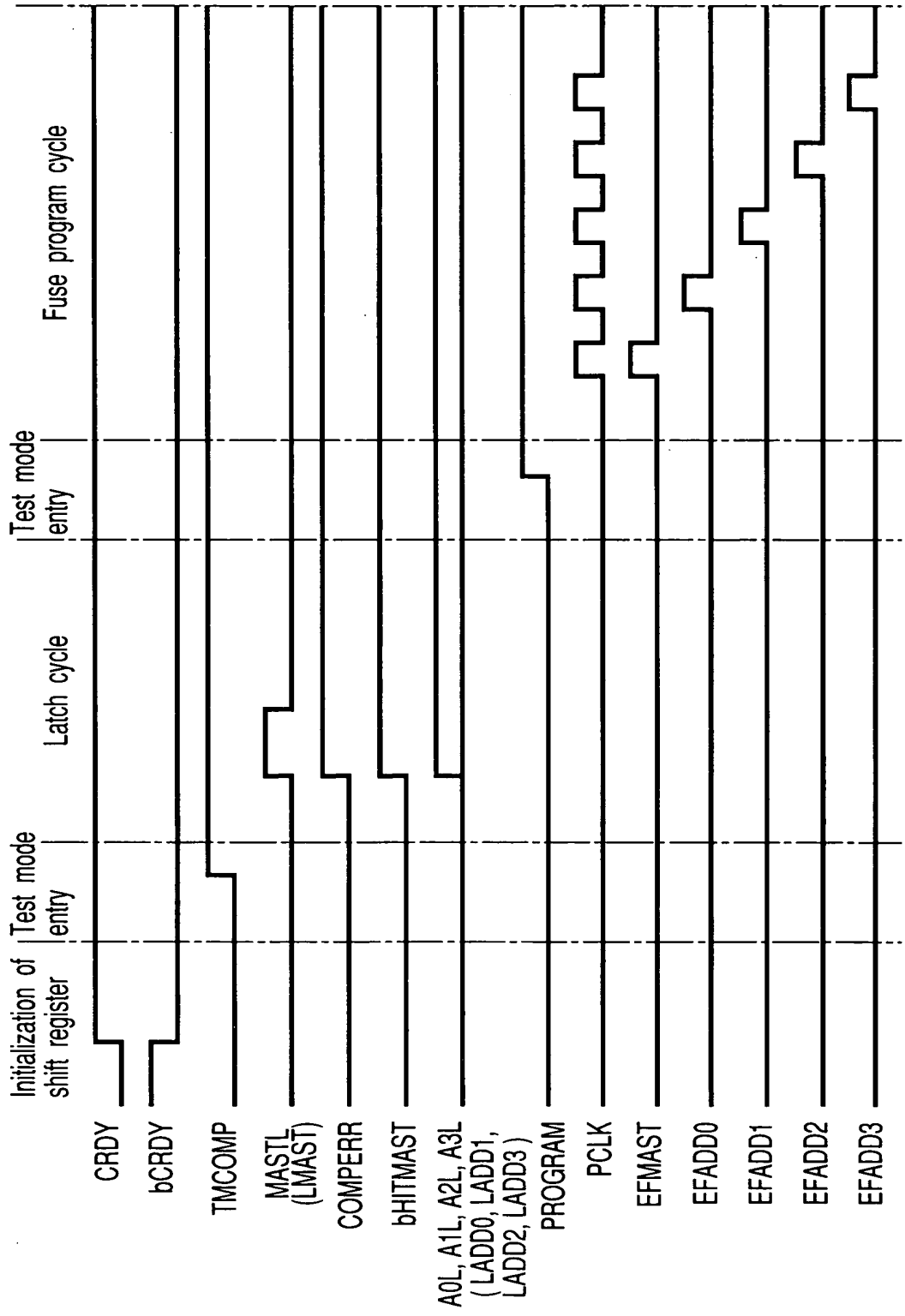
Initialization of shift register
Test mode entry
Latch cycle
Test mode entry
Fuse program cycle
CRDY
bCRDY
TMCOMP
MASTL (LMAST)
COMPERR
bHITMAST
A0L, A1L, A2L, A3L (LADD0, LADD1, LADD2, LADD3)
PROGRAM
PCLK
EFMAST
EFADD0
EFADD1
EFADD2
EFADD3

FIG. 28

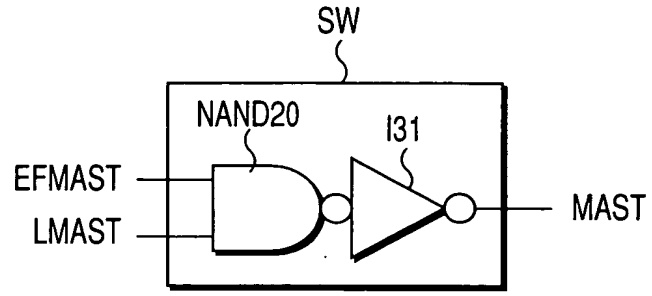

FIG. 29

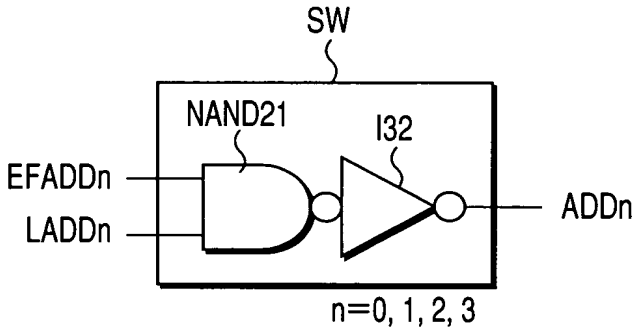

FIG. 30

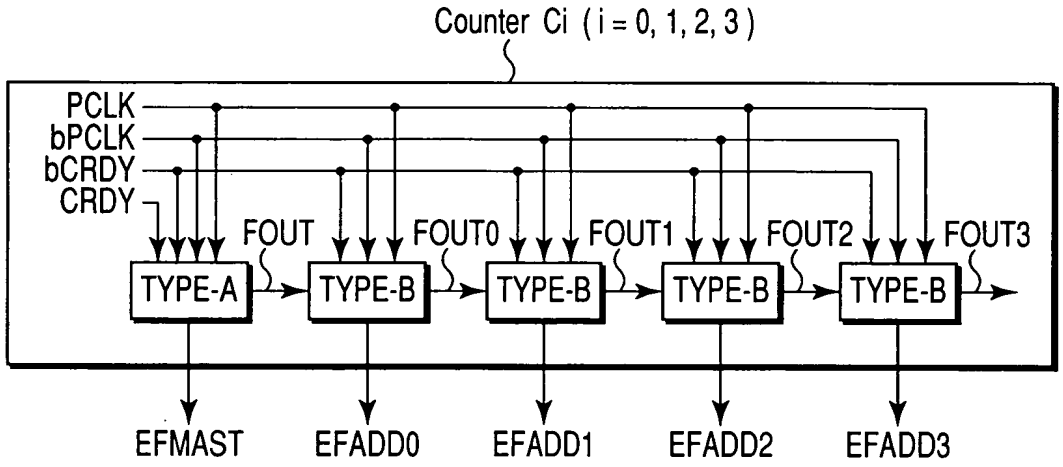

FIG. 31

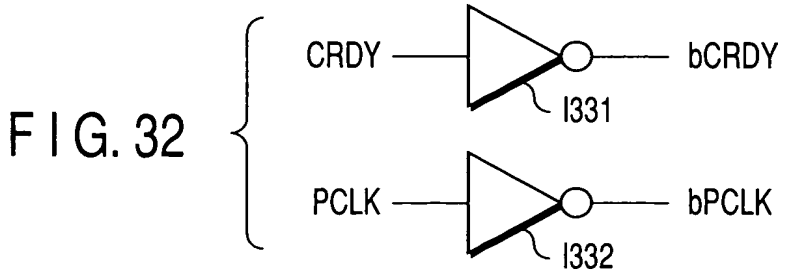

FIG. 32

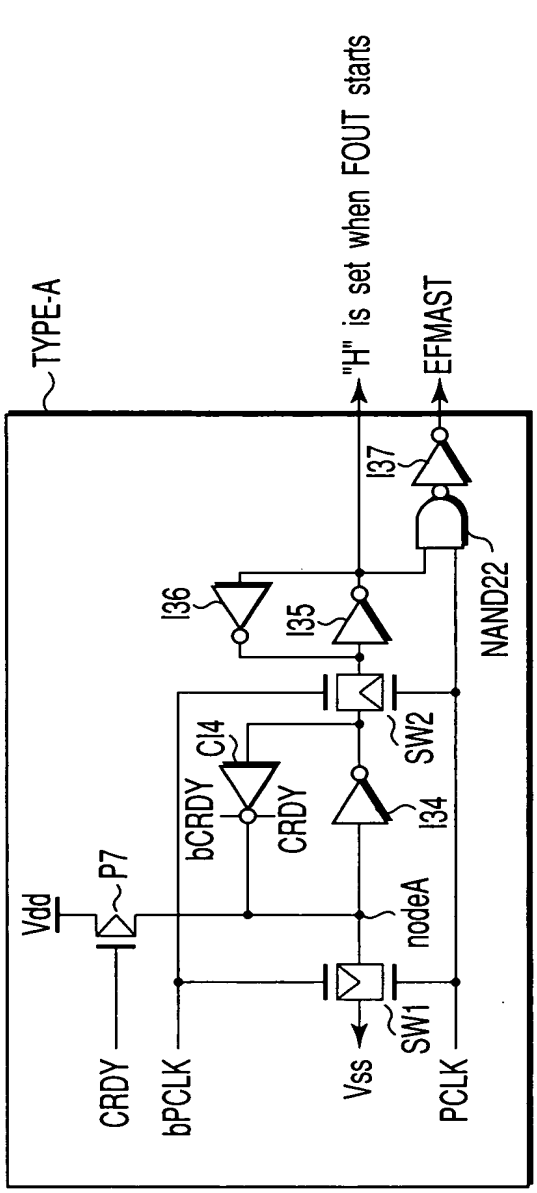
TYPE-A
"H" is set when FOUT starts
EFMAST
I37
NAND22
I36
I35
SW2
CI4
bCRDY
CRDY
I34
Vdd
P7
nodeA
SW1
CRDY
bPCLK
Vss
PCLK

FIG. 33

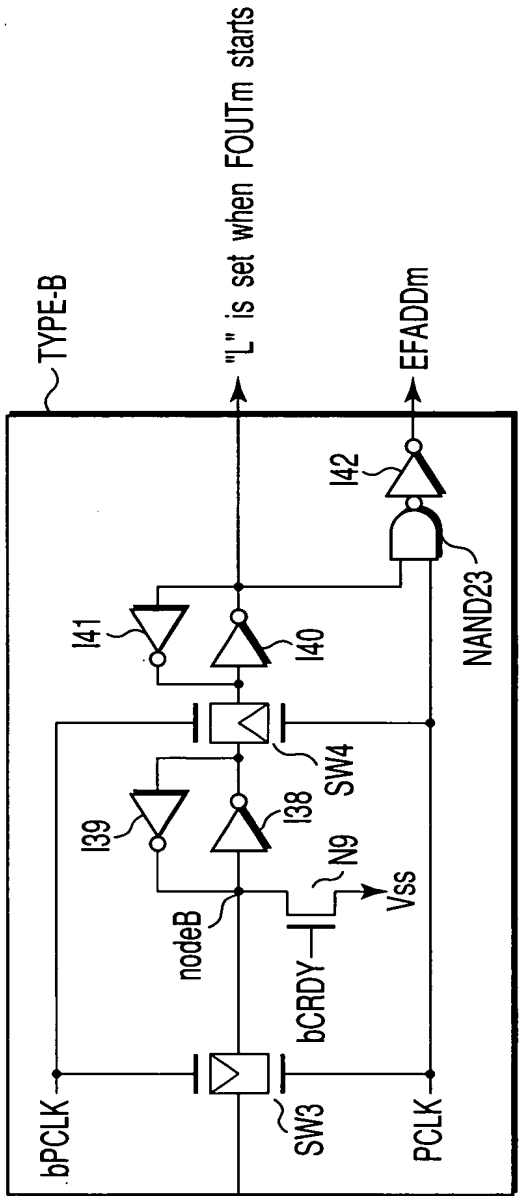
TYPE-B
"L" is set when FOUTm starts
EFADDm
I42
NAND23
I41
I40
SW4
I39
I38
N9
Vss
nodeB
bCRDY
SW3
bPCLK
PCLK
FINm
(FOUT, FOUTm-1)
m=0, 1, 2, 3

FIG. 34

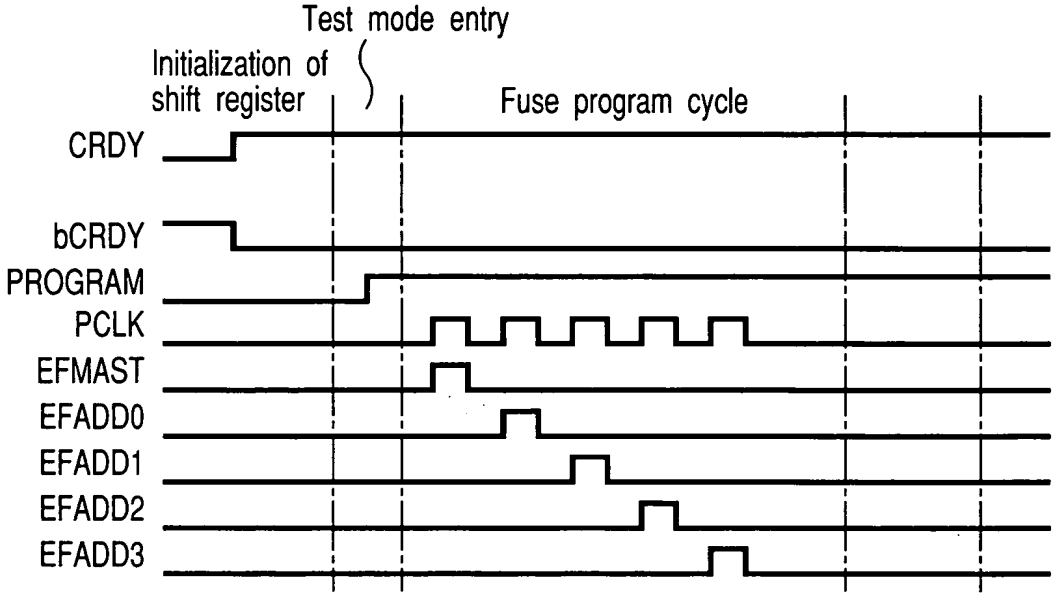
Test mode entry
Initialization of shift register
Fuse program cycle
CRDY
bCRDY
PROGRAM
PCLK
EFMAST
EFADD0
EFADD1
EFADD2
EFADD3

FIG. 35

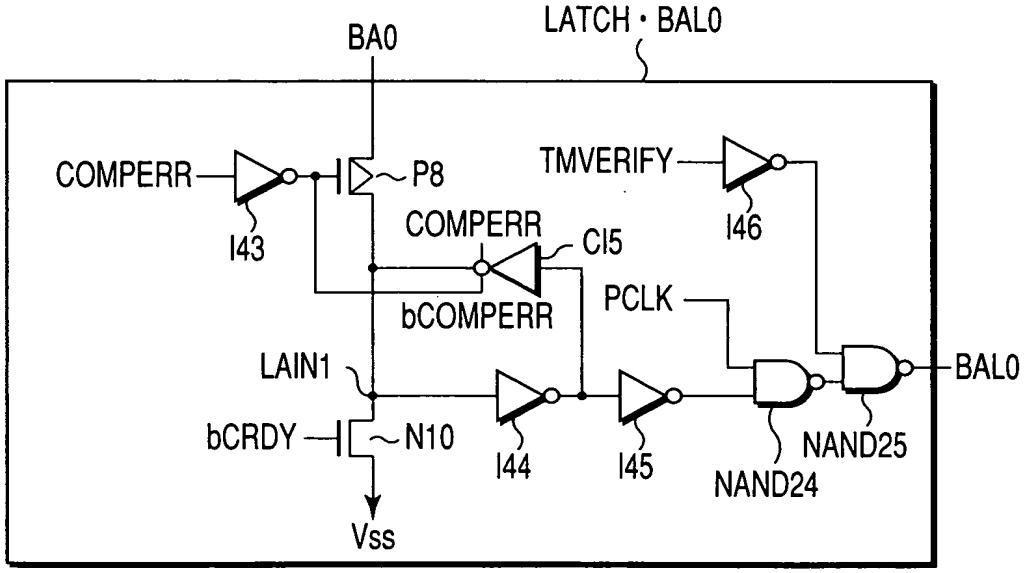
BA0
LATCH · BAL0
COMPERR
I43
P8
COMPERR
CI5
bCOMPERR
TMVERIFY
I46
PCLK
LAIN1
bCRDY
N10
I44
I45
NAND24
NAND25
BAL0
Vss

FIG. 36

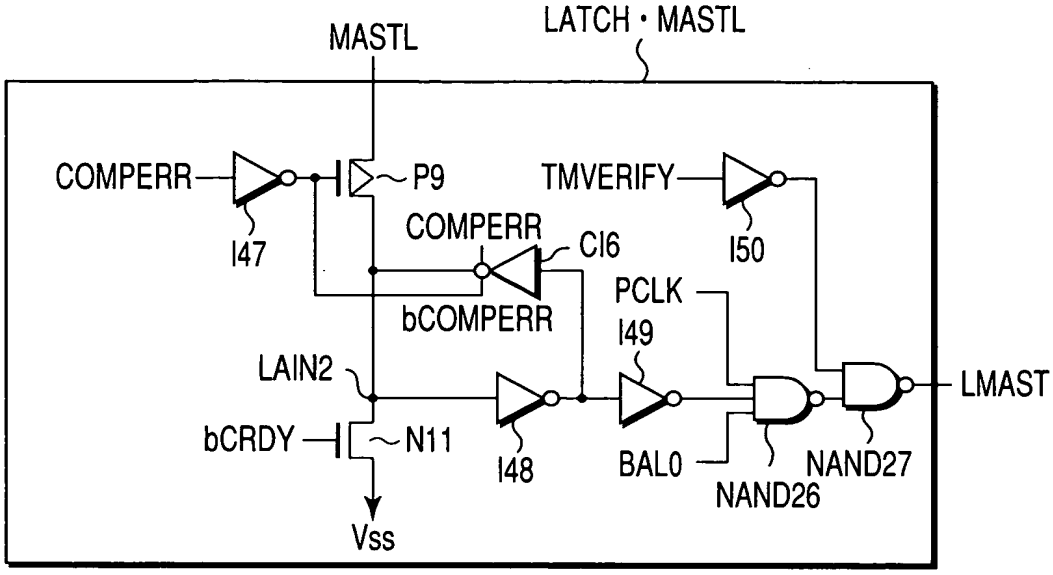
MASTL
LATCH · MASTL
COMPERR
P9
TMVERIFY
I47
COMPERR
CI6
I50
bCOMPERR
PCLK
I49
LAIN2
LMAST
bCRDY
N11
I48
BAL0
NAND27
NAND26
Vss

FIG. 37

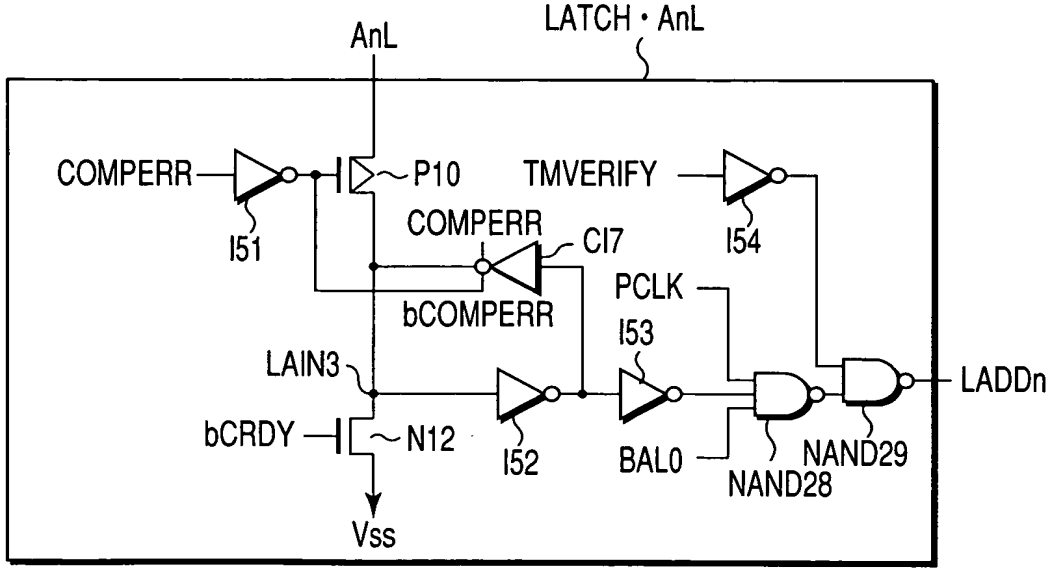
AnL
LATCH · AnL
COMPERR
P10
TMVERIFY
I51
COMPERR
CI7
I54
bCOMPERR
PCLK
I53
LAIN3
LADDn
bCRDY
N12
I52
BAL0
NAND29
NAND28
Vss

FIG. 38

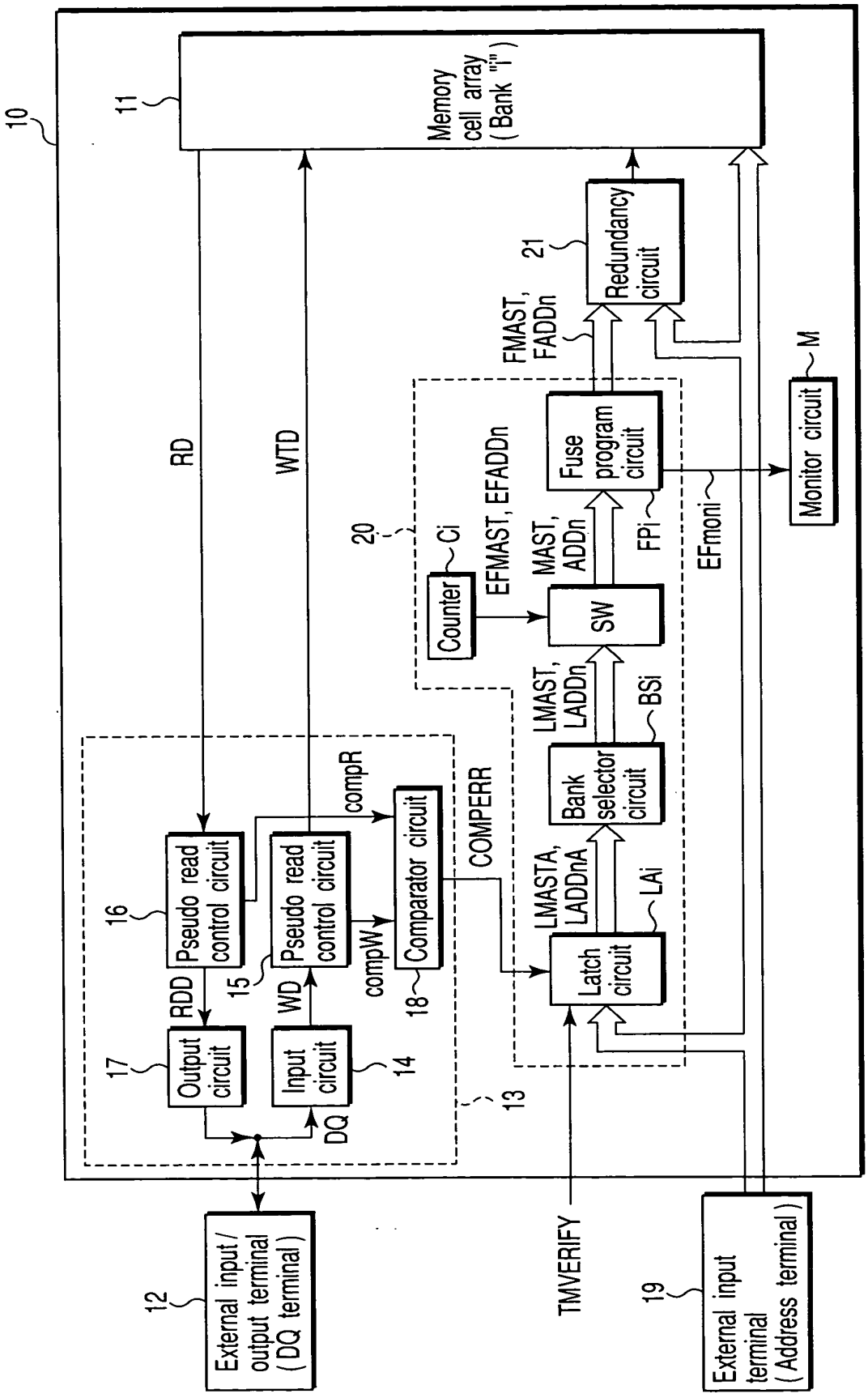
10
11
Memory cell array (Bank "i")
RD
WTD
21
Redundancy circuit
FMAST, FADDn
Fuse program circuit
M
Monitor circuit
20
Ci
Counter
EFMAST, EFADDn
MAST, ADDn
SW
FPi
EFmoni
LMAST, LADDn
BSi
Bank selector circuit
compR
COMPERR
Comparator circuit
16
Pseudo read control circuit
15
Pseudo read control circuit
compW
18
LMASTA, LADDnA
LAi
Latch circuit
RDD
17
Output circuit
WD
Input circuit
14
DQ
13
12
External input / output terminal (DQ terminal)
TMVERIFY
19
External input terminal (Address terminal)

FIG. 39

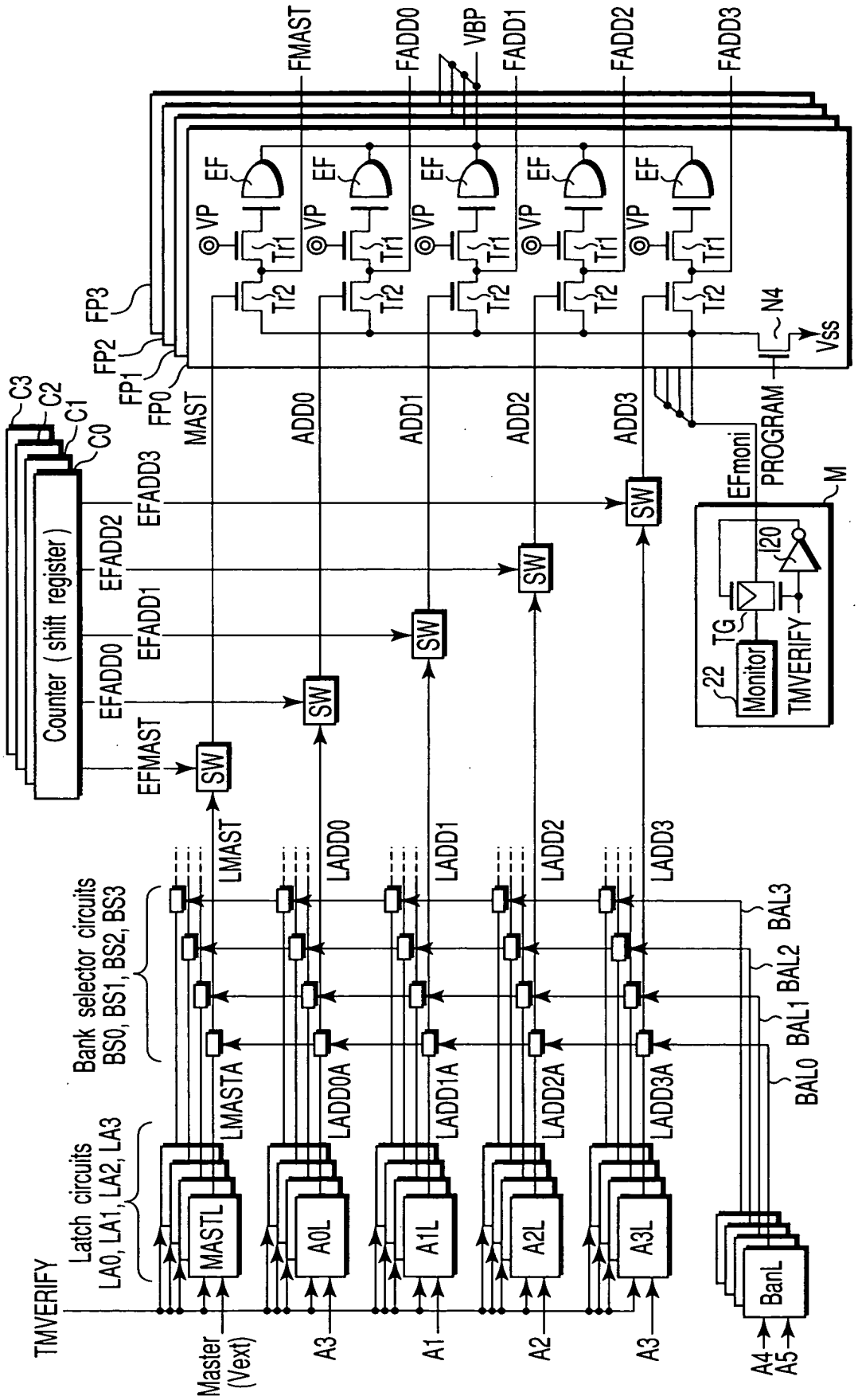
TMVERIFY
Latch circuits LA0, LA1, LA2, LA3
Bank selector circuits BS0, BS1, BS2, BS3
MASTL
A0L
A1L
A2L
A3L
BanL
LMASTA
LADD0A
LADD1A
LADD2A
LADD3A
LMAST
LADD0
LADD1
LADD2
LADD3
BAL0
BAL1
BAL2
BAL3
Master (Vext)
A3
A1
A2
A3
A4
A5
Counter (shift register)
C0
C1
C2
C3
EFMAST
EFADD0
EFADD1
EFADD2
EFADD3
SW
FP0
FP1
FP2
FP3
MAST
ADD0
ADD1
ADD2
ADD3
FMAST
FADD0
VBP
FADD1
FADD2
FADD3
EF
VP
Tr1
Tr2
N4
Vss
PROGRAM
EFmoni
M
I20
TG
22
Monitor
TMVERIFY

FIG. 40

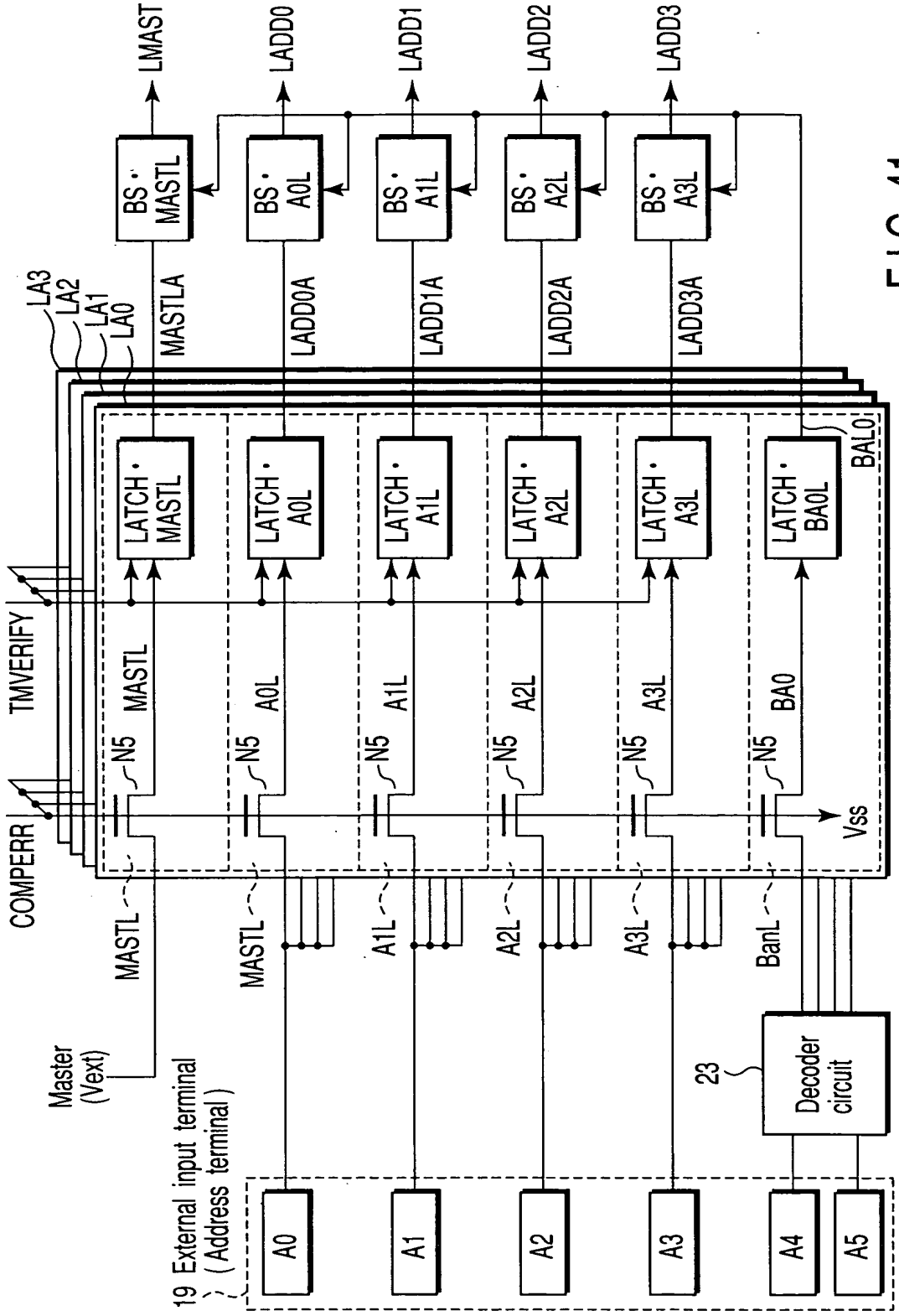
LMAST
LADD0
LADD1
LADD2
LADD3
BS · MASTL
BS · A0L
BS · A1L
BS · A2L
BS · A3L
LA3
LA2
LA1
LA0
MASTLA
LADD0A
LADD1A
LADD2A
LADD3A
LATCH · MASTL
LATCH · A0L
LATCH · A1L
LATCH · A2L
LATCH · A3L
LATCH · BA0L
BAL0
TMVERIFY
COMPERR
MASTL
A0L
A1L
A2L
A3L
BA0
N5
Vss
MASTL
MASTL
A1L
A2L
A3L
BanL
Master (Vext)
19 External input terminal (Address terminal)
23
Decoder circuit
A0
A1
A2
A3
A4
A5

FIG. 41

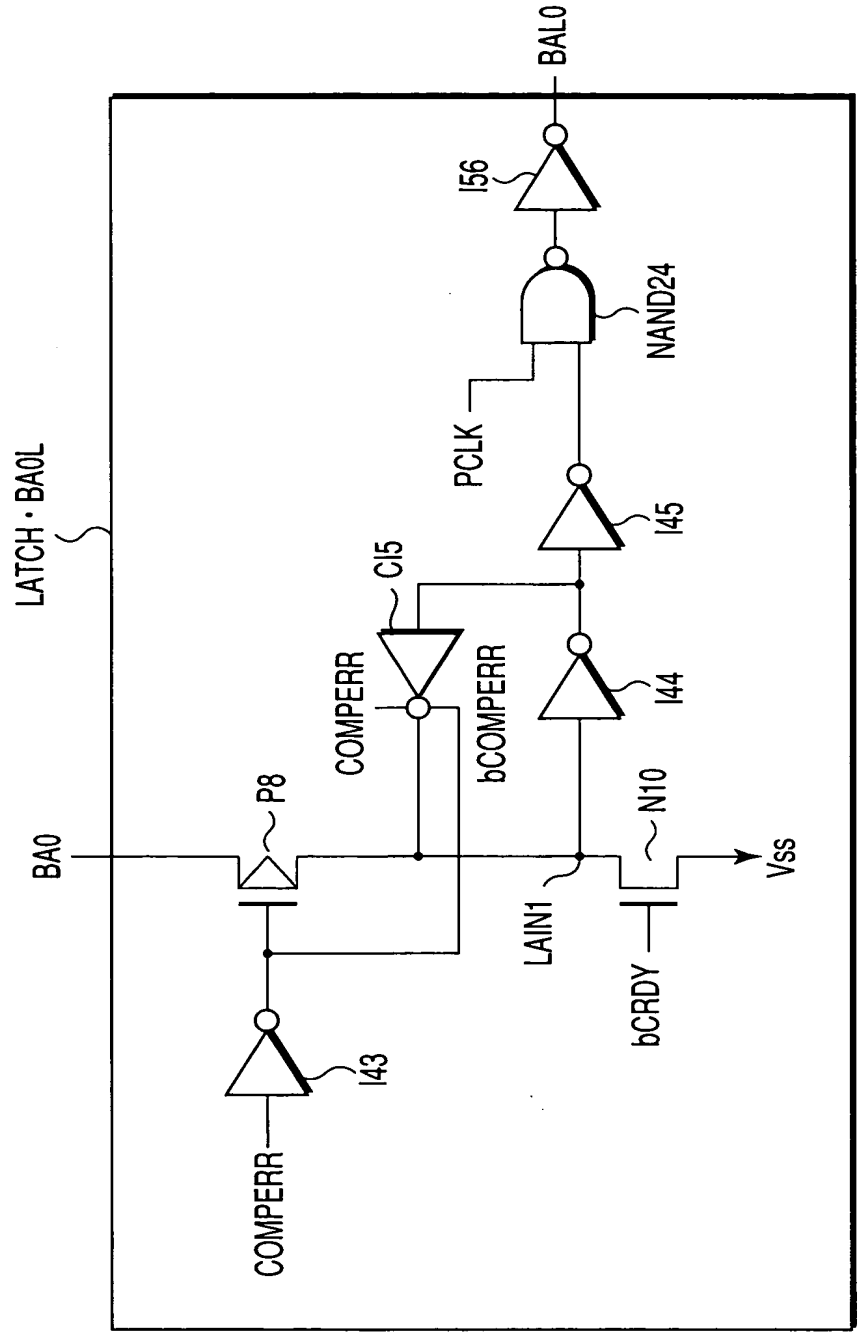
BAL0
I56
NAND24
PCLK
I45
CI5
COMPERR
bCOMPERR
I44
LATCH · BA0L
P8
N10
BA0
Vss
LAIN1
bCRDY
I43
COMPERR

FIG. 42

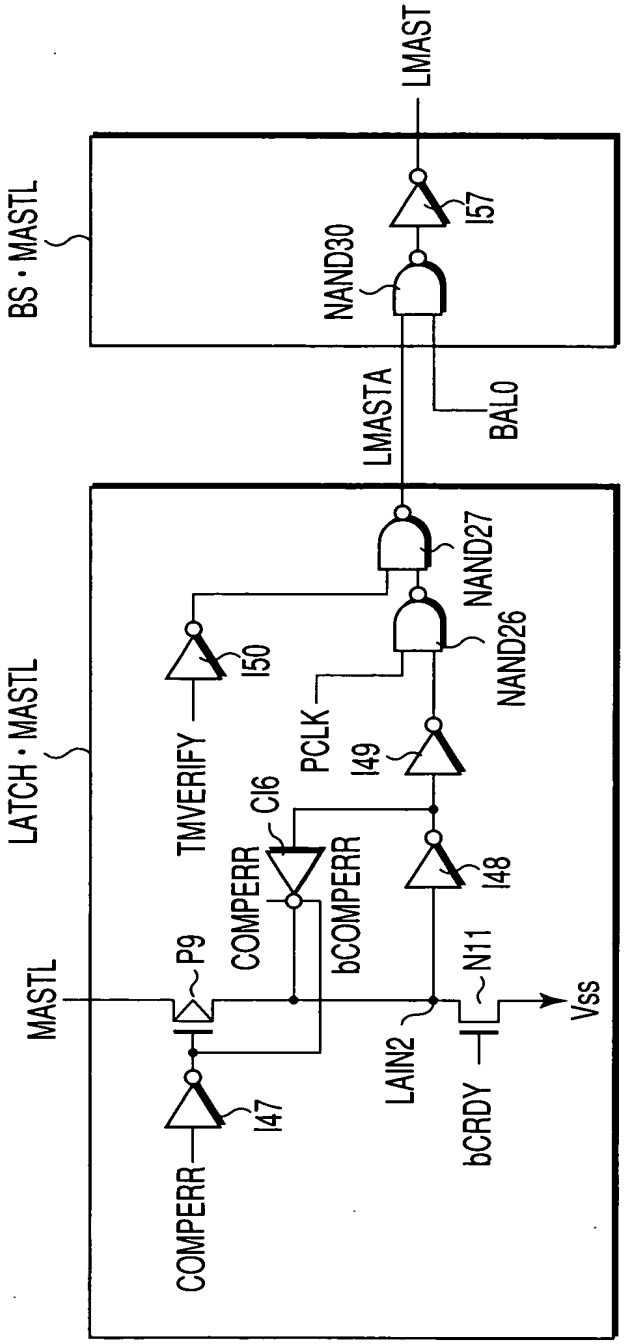
LMAST
BS • MASTL
I57
NAND30
LMASTA
BAL0
NAND27
NAND26
I50
TMVERIFY
PCLK
I49
LATCH • MASTL
CI6
COMPERR
bCOMPERR
I48
MASTL
P9
N11
Vss
LAIN2
bCRDY
I47
COMPERR

FIG. 43

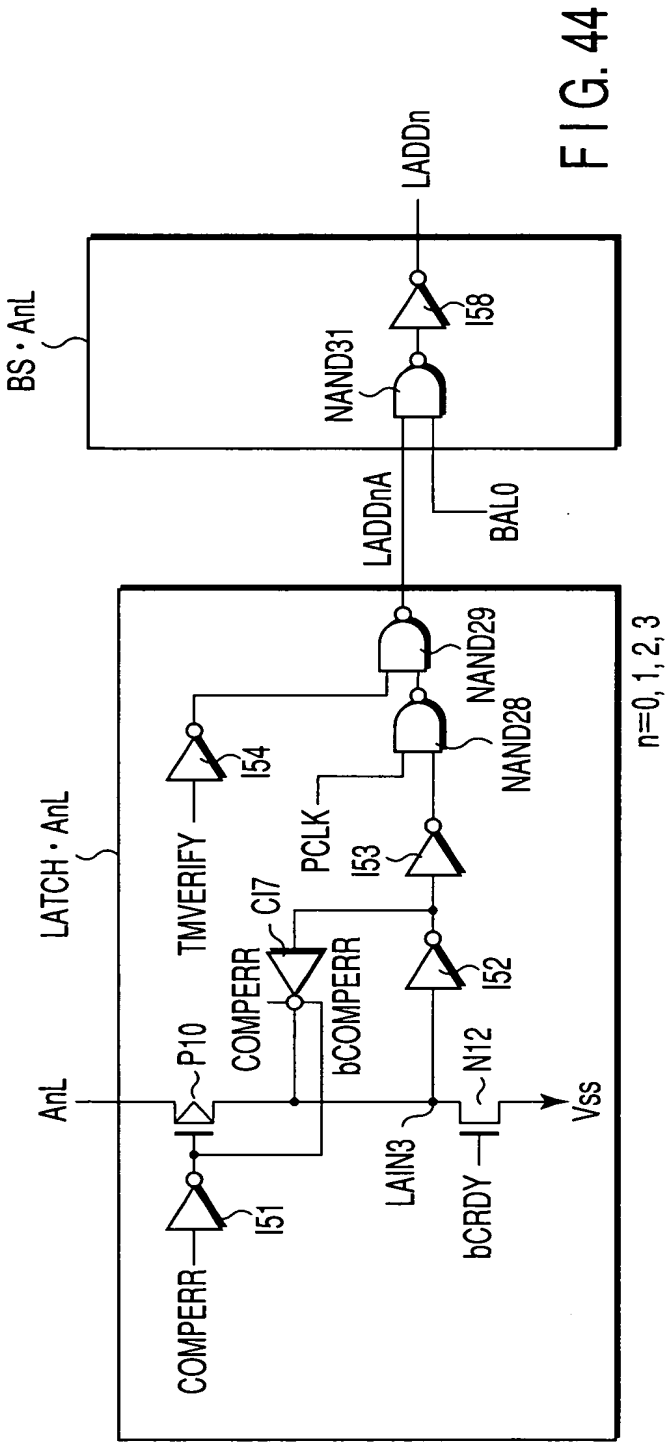
BS • AnL
LADDn
I58
NAND31
LADDnA
BAL0
LATCH • AnL
NAND29
NAND28
I54
TMVERIFY
PCLK
I53
CI7
COMPERR
bCOMPERR
I52
P10
N12
AnL
Vss
LAIN3
bCRDY
I51
COMPERR
n=0, 1, 2, 3

FIG. 44

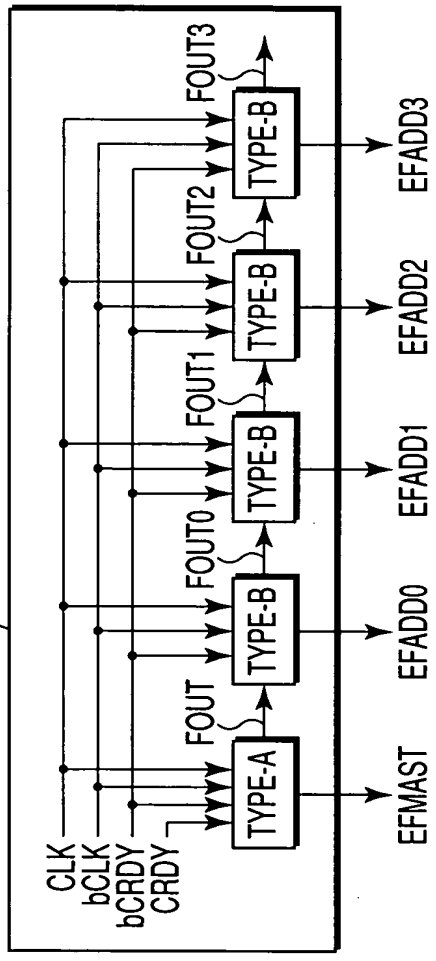
Counter Ci (i = 0, 1, 2, 3)
CLK
bCLK
bCRDY
CRDY
TYPE-A
TYPE-B
FOUT
FOUT0
FOUT1
FOUT2
FOUT3
EFMAST
EFADD0
EFADD1
EFADD2
EFADD3

FIG. 45

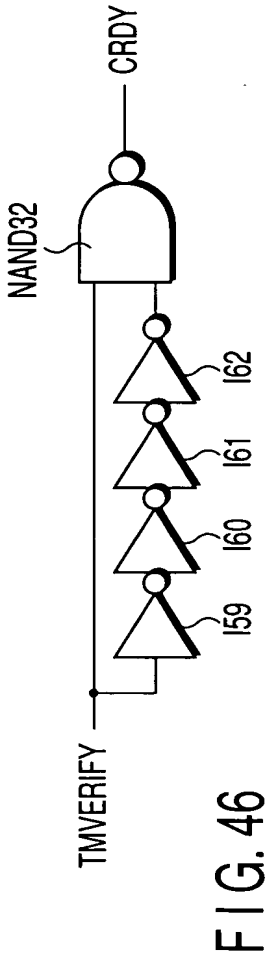

FIG. 46

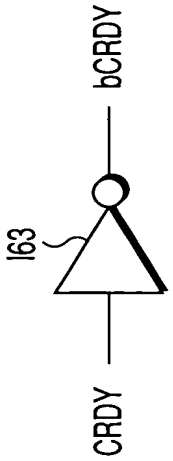

FIG. 47

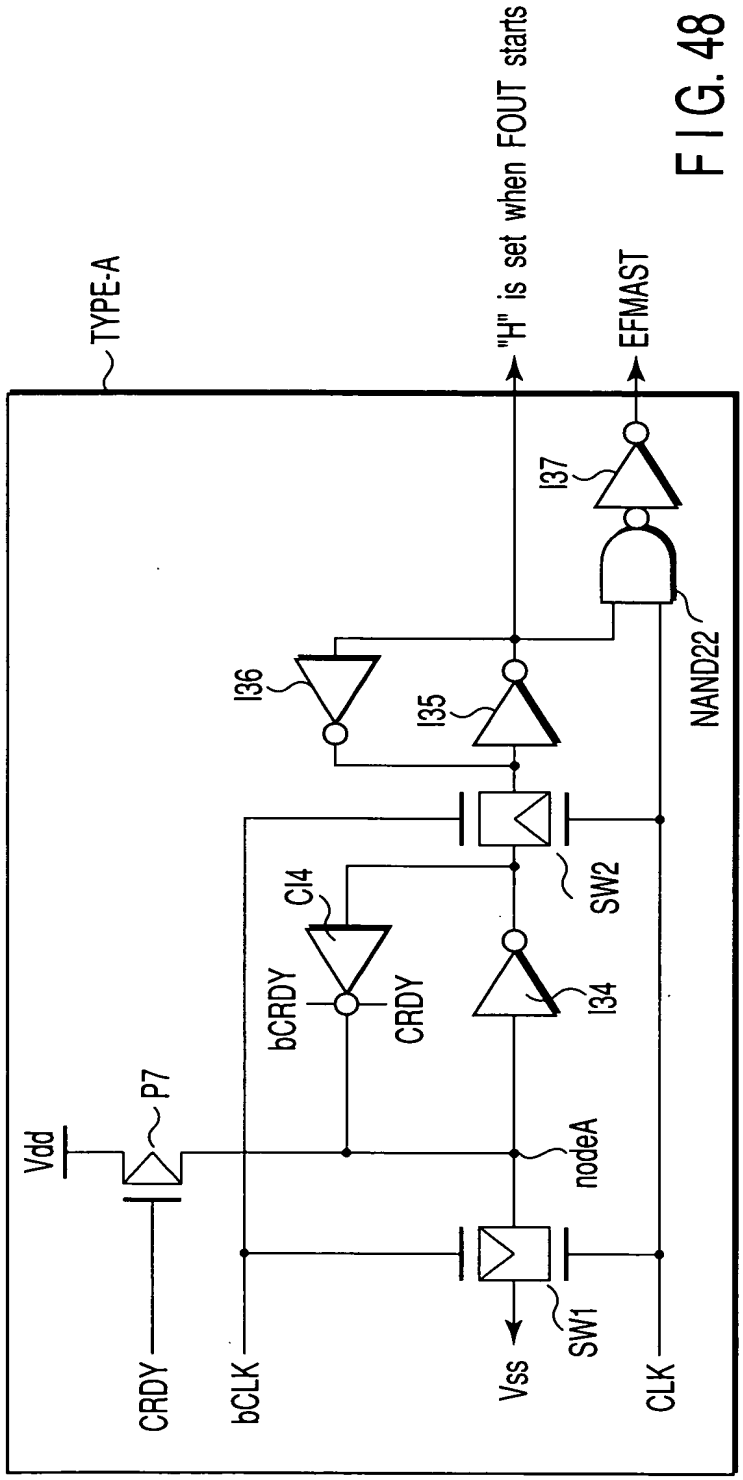

FIG. 48

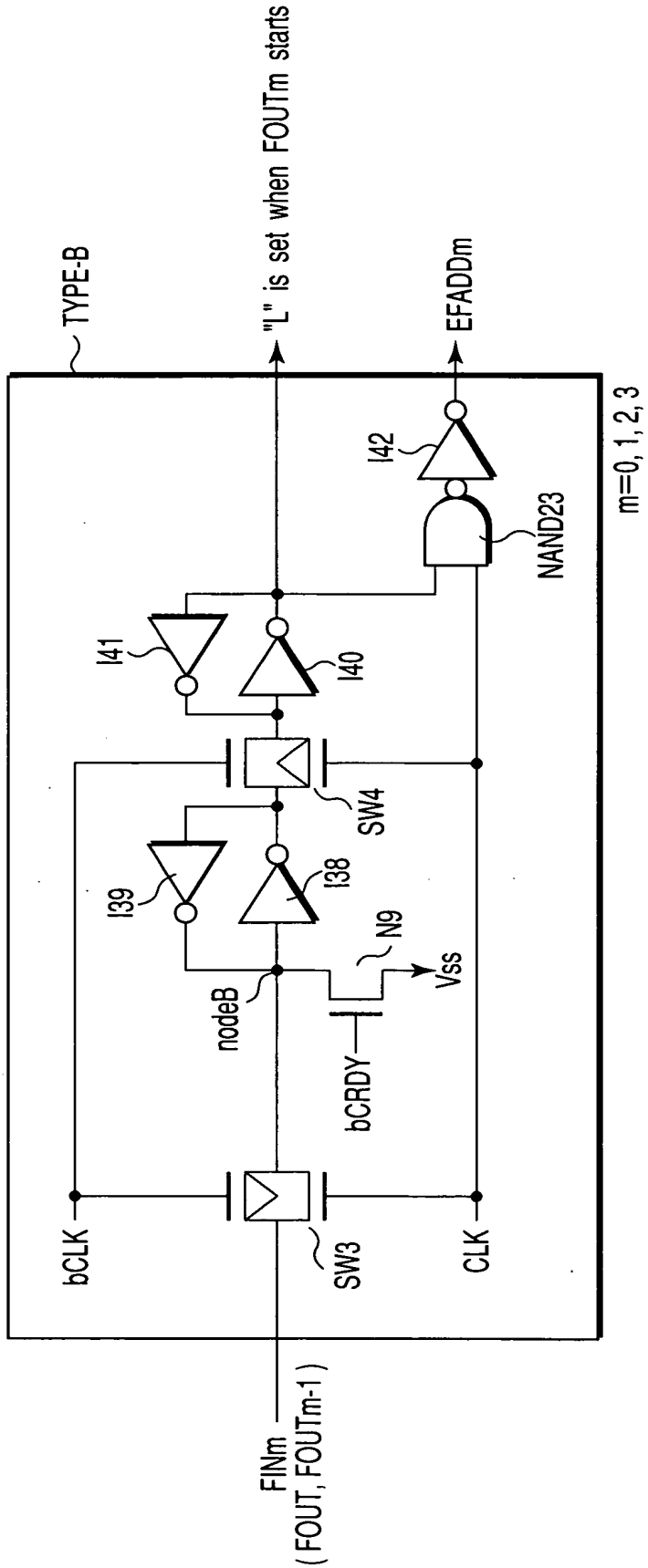
TYPE-B
"L" is set when FOUTm starts
EFADDm
I42
NAND23
m=0, 1, 2, 3
I41
I40
SW4
I39
I38
N9
Vss
nodeB
bCRDY
bCLK
SW3
CLK
FINm
(FOUT, FOUTm-1)

FIG. 49

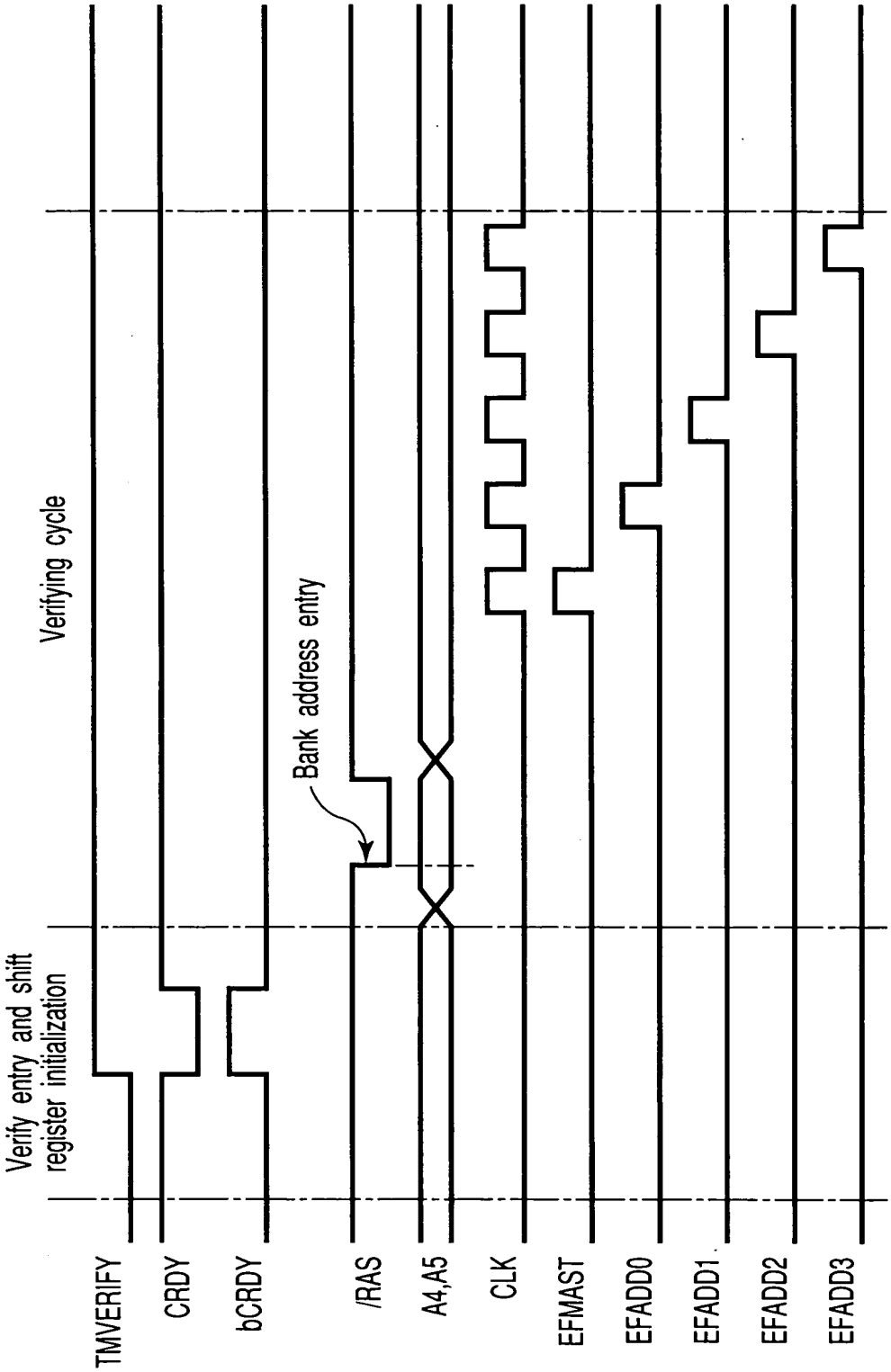
Verify entry and shift register initialization
Verifying cycle
Bank address entry
TMVERIFY
CRDY
bCRDY
/RAS
A4,A5
CLK
EFMAST
EFADD0
EFADD1
EFADD2
EFADD3

FIG. 50

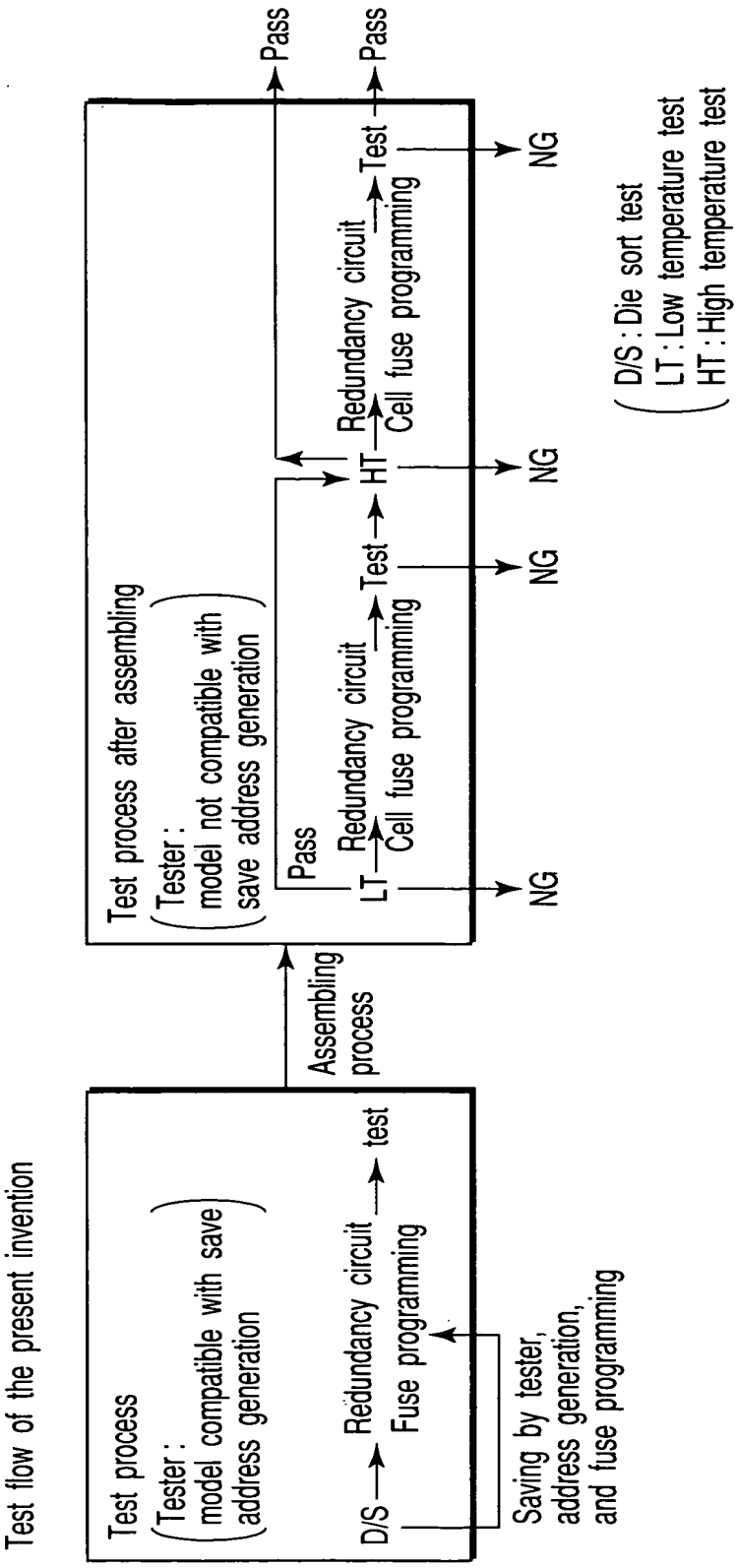
Test flow of the present invention
Test process
(Tester:
model compatible with save
address generation)
D/S
Redundancy circuit
Fuse programming
test
Saving by tester,
address generation,
and fuse programming
Assembling process
Test process after assembling
(Tester:
model not compatible with
save address generation)
LT
Pass
Redundancy circuit
Cell fuse programming
Test
NG
HT
Redundancy circuit
Cell fuse programming
Test
NG
Pass
NG
Pass
(D/S: Die sort test
LT: Low temperature test
HT: High temperature test

FIG. 51